A Low Power Single Phase Clock Distribution Using VLSI Technology

S.Indhumathi[1], S.Govindaraj[2],G. Selvaraj[3]

[1,2]*Assistant Professor, Department of Electronics and Communication*
[3]*Associate Professor & Head, Department of Mechanical Engineering*
Selvam College of Technology, Affiliated to Anna University, Chennai

Abstract- **The clock distribution network consumes nearly 70% of the total power consumed by the IC since this is the only signal which has the highest switching activity. Normally for a multi clock domain network we develop a multiple PLL to cater the need, this project aim for developing a low power single clock multiband network which will supply for the multi clock domain network. This project is highly useful and recommended for communication applications like Bluetooth, Zigbee. WLAN frequency synthesizers are proposed based on pulse-swallow topology and the designed is modeled using Verilog simulated using Modelsim and implemented in Xilinx**.

Keywords-Wideband E-TSPC Prescaler,Multimodulus Prescaler, Programmable Counter, Multiband Flexible Divide,.

I.INTRODUCTION

Wireless LAN (WLAN) in the multigigahertz bands such as HiperLAN II and IEEE 802.11a/b/g, are recognized as leading standards for high-rate data transmissions, and standards like IEEE802.15.4 are recognized for low-rate data transmissions. The demand for lower cost, lower power, and multiband RF circuits increased in conjunction with need of higher level of integration. The frequency synthesizer, usually implemented by a phase-locked loop (PLL), is one of the power-hungry blocks in the RF front-end and the first stage frequency divider consumes a large portion of power in frequency synthesizer. The integrated synthesizers for WLAN applications at 5 GHz consume up to 25 mW in CMOS realizations, where the first-stage divider is implemented using an injection-locked divider which consumes large chip area and has a narrow locking range.

The best published frequency synthesizer at 5 GHz consumes 9.7 mWat 1V supply, where its complete divider consumes power around 6 mW, where the first-stage divider is implemented using the source-coupled logic (SCL) circuit which allows higher operating frequencies but uses more power. Dynamic latches are faster and consume less power compared to static dividers. The TSPC and E-TSPC designs are able to drive the dynamic latch with a single clock phase and avoid the skew problem. However, the adoption of single-phase clock latches in frequency dividers has been limited to PLLs with applications below 5 GHz .

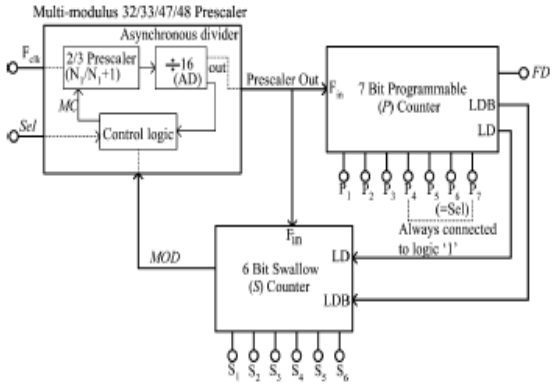

Fig.1.Proposed dynamic logic multiband flexible Divider.

The frequency synthesizer uses an E-TSPC prescaler as the first-stage divider, but the divider consumes around 6.25 mW. Most IEEE 802.11a/b/g frequency synthesizers employ SCL dividers as their first stage while dynamic latches are not yet adopted for multiband synthesizers.

In this paper, a Dynamic logic multiband flexible integer-n divider based on pulse-swallow topology is proposed which uses a low-power wideband 2/3 prescaler and a wideband multimodulus 32/33/47/48 prescaler as shown in Fig.1 The divider also uses an improved low power loadable bit-cell for the Swallow S-counter.

A.DESIGN CONSIDERATIONS

The key parameters of high-speed digital circuits are the propagation delay and power consumption. The maximum operating frequency of a digital circuit is calculated and is given by

$$f_{max} = 1/t_{pLH}+t_{pHL} \qquad (1)$$

Where t_{pLH} and t_{pHL} are the propagation delays of gates, respectively. The total power consumption of the CMOS digital circuits is determined by the switching and short circuit power. The switching power is linearly

proportional to the operating frequency and is given by the sum of switching power at each output node as in

$$P_{switching} = \sum f_{clk} C_{Li} V^2_{dd} \quad (2)$$

Where n is the number of switching nodes, f_{clk} is the clock frequency, C_{Li} the load capacitance at the output node of the ith stage, and v_{dd} is the supply voltage. Normally the short-circuit power occurs in dynamic circuits when there exists direct paths from the supply to ground which is given by

$$P_{SC}=I_{SC}*v_{dd} \quad (3)$$

Where I_{SC} is the short-circuit current. The analysis in E-TSPC shows that the short-circuit power is much higher in E-TSPC logic circuits than in TSPC logic circuits. However, TSPC logic circuits exhibit higher switching power compared to that of E-TSPC logic circuits due to high load capacitance. For the E-TSPC logic circuit, the short-circuit power is the major problem.

The E-TSPC circuit has the merit of higher operating frequency than that of the TSPC circuit due to the reduction in load capacitance, but it consumes significantly more power than the TSPC circuit does for a given transistor size. The following analysis is based on the latest design using the popular and low-cost 0.18µ CMOS process.

II. WIDEBAND E-TSPC 2/3 PRESCALER

The E-TSPC 2/3 prescaler consumes large short circuit power and has a higher frequency of operation than that of TSPC 2/3 prescaler. The wideband single-phase clock 2/3 prescaler used in this design consists of two D-flip-flops and two NOR gates embedded in the flip-flops as in Fig. 2.

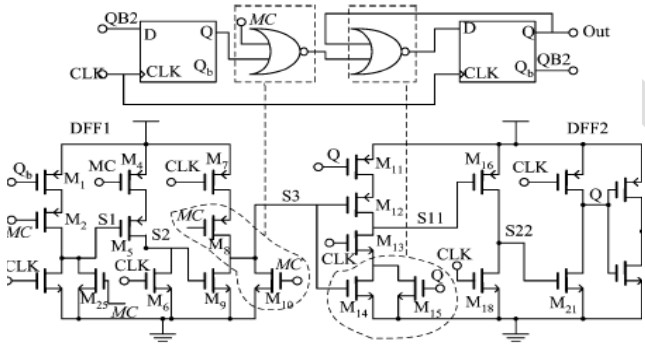

Fig.2. Wideband Single phase Clock 2/3 Prescaler.

The first NOR gate is embedded in the last stage of DFF1, and the second NOR gate is embedded in the first stage of DFF2 . Here, the transistors M_2, M_{25},M_4,M_8 in DFF1 helps to eliminate the short-circuit power during the divide-by-2 operation. The switching of division ratios between 2 and 3 is controlled by logic signal MC. The load capacitance of the prescaler is given by

$$C_{L\text{-}wideband}=C_{dbM19}+2C_{gdM19}+C_{dbM21}+2C_{gdM21}+C_{Gm1} \quad (1)$$

When MC switches from "0" to "1," transistors M_2,M_4 and M_8 in DFF1 turns off and nodes S1, S2 and S3 switch to logic "0." Since node S3 is "0" and the other input to the NOR gate embedded in DFF2 is Qb, the wideband prescaler operates at the divide-by-2 mode. During this mode, nodes S1, S2 and S3 switch to logic "0" and remain at "0" for the entire divide-by-2 operation, thus removing the switching power contribution of DFF1. Since one of the transistors is always OFF in each stage of DFF1, the short-circuit power in DFF1 and the first stage of DFF2 is negligible. The total power consumption of the prescaler in the divide-by-2 mode is equal to the switching power in DFF2 and the short-circuit power in second and third stages of DFF2 and is given by

$$P_{widebanb\text{-}divide\text{-}by\text{-}2}=\sum f_{clk} C_{Li} v^2_{dd+} P_{SC1+} P_{SC2} \quad (2)$$

Where C_{Li} is the load capacitance at the output node of the ith stage of DFF2, and P_{SC1} and P_{SC2} are the short-circuit power in the second and third stages of DFF2. When logic signal MC switches from "1"to "0," the logic value at the input of DFF1 is transferred to the input of DFF2 as one of the input of the NOR gate embedded in DFF1 is "0" and the wideband prescaler operates at the divide-by-3 mode. During the divide-by-2 operation, only DFF2 actively participates in the operation and contributes to the total power consumption since all the switching activities are blocked in DFF1. Thus, the wideband 2/3 prescaler has benefit of saving more than 50% of power during the divide-by-2 operation. The measured results shows that the wideband 2/3 prescaler has the maximum operating frequency of 6.5GHz.

III.MULTIMODULUS 32/33/47/48 PRESCALER

The proposed wideband multimodulus prescaler which can divide the input frequency by 32, 33, 47, and 48 is shown in Fig.3. It is similar to the 32/33 prescaler but with an additional inverter and a multiplexer. The proposed prescaler performs additional divisions (divide-by-47 and divide-by-48) without any extra flip-flop, thus saving a considerable amount of power and also reducing the complexity of multiband divider.

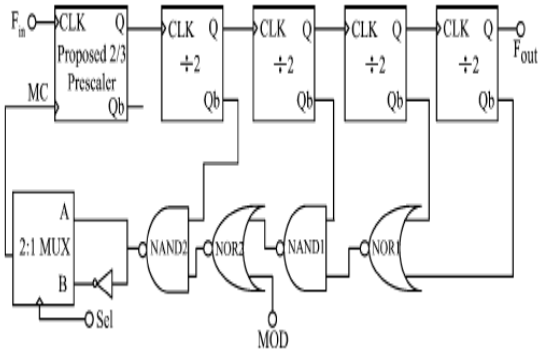

Fig.3. Proposed Multimodulus 32/33/47/48 Prescaler.

The multimodulus prescaler consists of the wideband 2/3 ($N_1/(N_1+1)$) prescaler, four asynchronous TSPC divide-by-2 circuits ((AD)=16) and combinational logic circuits to achieve multiple division ratios. Beside the usual MOD signal for controlling N/(N+1) divisions, the additional control signal sel is used to switch the prescaler between 32/33and 47/48 modes.

1) Case 1: sel='0'

When sel='0', the output from the NAND2 gate is directly transferred to the input of 2/3 prescaler and the multimodulus prescaler operates as the normal 32/33 prescaler, where the division ratio is controlled by the logic signal MOD. If MC=1, the 2/3 prescaler operates in the divide-by-2 mode and when MC=0, the 2/3 prescaler operates in the divide-by-3 mode. If MOD=1, the NAND2 gate output switches to logic "1" (MC=1) and the wideband prescaler operates in the divide-by-2 mode for entire operation. The division ratio N performed by the multimodulus prescaler is

$$N=(AD*N_1)+(0*(N_1+1))=32 \quad (1)$$

Where $N_1=2$ and AD=16 is fixed for the entire design. If MOD=0 , for 30 input clock cycles MC remains at logic "1", where wideband prescaler operates in divide-by-2 mode and, for three input clock cycles, MC remains at logic "0" where the wideband prescaler operates in the Divide-by-3 mode. The division ratio N+1 performed by the multimodulus prescaler is

$$N+1=((AD-1)*N_1) \quad (2)$$

2) Case 2**:**sel ='1'

When sel='1', the inverted output of the NAND2 gate is directly transferred to the input of 2/3 prescaler and the multimodulus prescalar operate as a 47/48 prescaler, where the division ratio is controlled by the logic signal MOD. If MC=1, the 2/3 prescaler operates individe-by-3 mode and when MC=0, the 2/3 prescaler operates individe-by-2 mode which is quite opposite to the operation performed when sel='0' If MOD=1, the division ratio N+1 performed by the multimodulus prescaler is same except that the wideband prescaler operates in the divide by-3 mode for the entire operation given by

$$N+1=(AD*(N1+1))+(0*N1)=48 \quad (3)$$

If MOD=1, the division ratio N performed by the multimodulus prescaler is

$$N=((AD-1)*(N1+1))+(1*N1)=47 \quad (4)$$

IV MULTIBAND FLEXIBLE DIVIDER

The single-phase clock multiband flexible divider which is shown in Fig1.1 consists of the multimodulus 32/33/47/48 prescaler, a 7-bit programmable P-counter and a 6 bit swallow S-counter. The control signal Sel decides whether the divider is operating in lower frequency band (2.4 GHz) or higher band (5–5.825 GHz).

A.Swallow (S) Counter

The 6-bit s-counter shown in Fig.4. consists of six asynchronous loadable bit-cells, a NOR-embedded DFF and additional logic gates to allow it to be programmable from 0 to 31 for low-frequency band and from 0 to 47 for the high-frequency band. The asynchronous bit cell used in this design shown in Fig.4. is similar to the bit-cell except it uses two additional transistors M_6 and M_7whose inputs are controlled by the logic signal MOD. If MOD is logically high, nodes S1 and S2 switch to logic "0" and the bit-cell does not perform any function. The MOD signal goes logically high only when the S-counter finishes counting down to zero. If MOD and LD are logically low, the bit-cell acts as a divide-by-2 unit. If MOD is logically low and LD is logically high, the input bit PI is transferred to the output.

In the initial state, MOD=0, the multimodulus prescaler selects the divide-by-N+1 mode (divide-by-33 or divide-by-48) and P, S counters start down counting the input clock cycles. When the S-counter finishes counting, MOD switches to logic "1" and the prescaler changes to the divide-by-n mode (divide-by-32 or divide-47) for the remaining P-S clock cycles. During this mode, since S-counter is idle, transistors M_6 and M_7 which are controlled by MOD, keep the nodes S1 and S2 at logic "0," thus saving the switching power in S-counter for a period of (N*(P-S)) clock cycles. Here, the programmable input (PI) is used to load the counter to a specified value from 0 to 31 for the lower band and 0 to 48 for the higher band of operation.

B. Programmable (P) Counter

The programmable P-counter is a 7-bit asynchronous down counter which consists of 7 loadable bit-cells and additional logic gates. Here, bit P_7 is tied to the Sel signal of the multi modulus prescaler and bits P_4 and P_7 are always at logic "1." The remaining bits can be externally programmed from 75 to 78 for the lower frequency band and from 105 to 122 for the upper frequency band. When the P-counter finishes counting down to zero, LD switches to logic "1" during which the output of all the bit-cells in S-counter switches to logic "1" and output of the NOR embedded DFF switches to logic "0" (MOD=0) where the programmable divider get reset to its initial state and thus a fixed division ratio is achieved. If a fixed 32/33 (N/(N+1)) dual-modulus prescaler is used, a 7bit P-counter is needed for the low-frequency band (2.4 GHz) while an 8-bit S-counter would be needed for the high frequency band(5–5.825 GHz) with a fixed 5-bit S-counter. Thus, the multimodulus32/33/47/48 prescaler eases the design complexity of the P-counter.

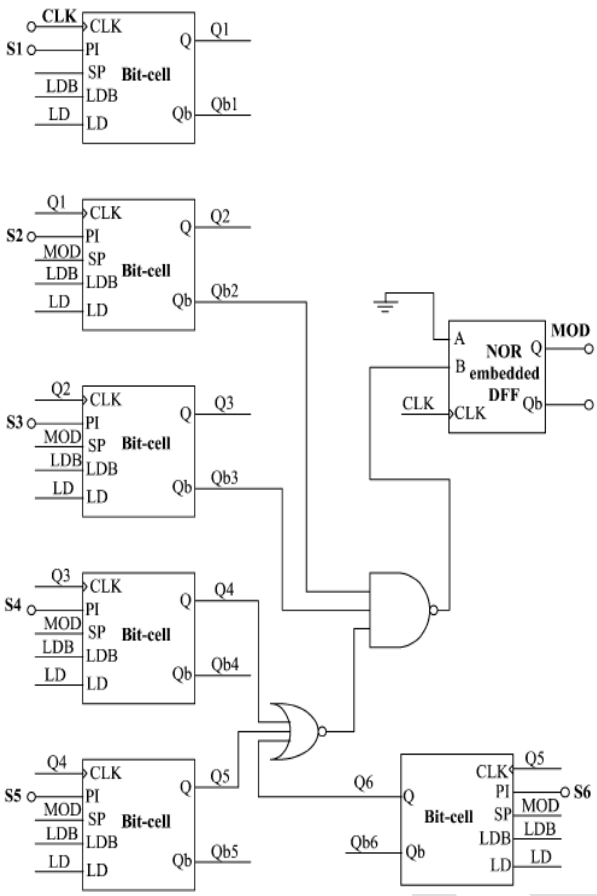

Fig..4. Asynchronous 6-Bit S-Counter.

V .RESULTS AND CONCLUSION

A.PRESCALER FREQUENCY DIVIDE RATIOS

TABLEI
PRESCALERFREQUENCYDIVIDERATIOS

Sel	MOD	MC	MODE
0	1	1	Divide-by-2
	0	1	Divide-by-2
	0	0	Divide-by-3
1	1	0	Divide-by-2
		1	Divide-by-3

1)When Sel='0':

When Sel='0' the output from N4 gate is given to the prescaler and the multimodulus prescaler selects 32/33 mode and the division ratio is controlled by MOD signal. When MOD=1 the output from N4 gate switches to logic '1' and the prescaler operates in divide-by-2 for entire operation. i.e., now division ratio of 32 (N) is performed. Similarly when MOD=0, MC remains high for first 30 input clock cycles and goes low for 3 input clock cycles. Thus division ratio of 33(N+1) is performed. N and N+1 are given by

$$N = (AD * N1) = 32$$
$$N+1 = ((AD-1) * N1) + (1*(N1+1)) = 33$$

2)When Sel=1:

When Sel=1, the inverted output from N4 gate is given to the input of 2/3 prescaler and multimodulus prescaler operates in 47/48 mode. MOD signal controls the division ratio. When MOD=1 and MC=1 prescaler operated in divide-by-3 for the entire input cycles and division ratio of 48(N+1) is performed. When MOD=1 and MC=0 divideby-2 is selected for entire input clock cycles for prescaler and the division ratio of 47(N) is performed. N and N+1 are given by

$$N = ((AD-1) * (N1+1)) + (1 * N1) = 47$$
$$N+1 = (AD * (N1+1)) = 48$$

B.SIMULATED ENVIRONMENT

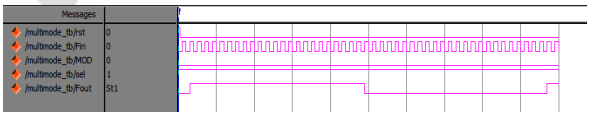

Fig.5.DIVIDE-BY-32

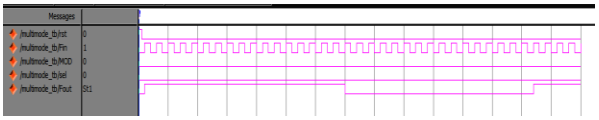

Fig.6.DIVIDE-BY-33

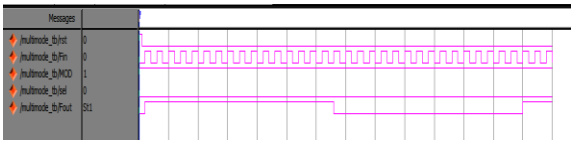

Fig.7.DIVIDE-BY-47

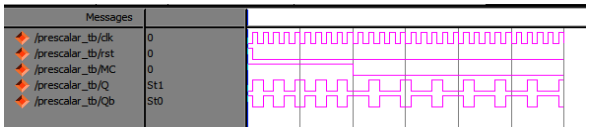

Fig.8. PRESCALER 2/3

V.CONCLUSION

In this paper a simple approach for the low power single phase clock distribution for Wireless Local Area Networks frequency synthesizer is presented. The technique for low power fully programmable divider using design of reloadable bit cells for P and S Counter is given. P and S counters can be programmed accordingly for the required bands of frequencies. Here the clock divider uses a wide band 2/3 prescaler and a multimodulus prescaler. By using this multimodulus prescaler, the Clock Jitter can be avoided.

REFERENCE

[1] H.R.Rategh *et al.*, "A CMOS frequency synthesizer with an injectedlocked frequency divider for 5-GHz wirless LAN receiver," *IEEE J. Solid-State Circuits*, vol. 35, no. 5, pp. 780–787, May 2000.

[2] P. Y. Deng *et al.*, "A 5 GHz frequency synthesizer with an injection locked frequency divider and differential switched capacitors," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 56, no. 2, pp. 320–326, Feb. 2009.

[3] L. Lai Kan Leung *et al.*, "A 1-V 9.7-mW CMOS frequency synthesizer for IEEE 802.11a transceivers," *IEEE Trans. Microw. Theory Tech.*, vol. 56, no. 1, pp. 39–48, Jan. 2008.

[4] M. Alioto and G. Palumbo, *Model and Design of Bipolar and MOS Current-Mode Logic Digital Circuits*. New York: Springer, 2005.

[5] Y. Ji-ren *et al.*, "Atrue single-phase-clock dynamicCMOScircuit technique," *IEEE J. Solid-State Circuits*, vol. 24, no. 2, pp. 62–70, Feb. 1989.

[6] S. Pellerano *et al.*, "A 13.5-mW 5 GHz frequency synthesizer with dynamic-logic frequency divider," *IEEE J. Solid-State Circuits*, vol. 39, no. 2, pp. 378–383, Feb. 2004.

[7] V. K. Manthena *et al.*, "A low power fully programmable 1 MHz resolution 2.4 GHz CMOS PLL frequency synthesizer," in *Proc. IEEE Biomed. Circuits Syst. Conf.*, Nov. 2007, pp. 187–190.

Indhumathi S received the BE degree in Electronics and Communication Engineering from Anna University-Trichy in 2011. She received the ME degree in VLSI Design from Anna University-Chennai in 2013.
She has one year of teaching experience in Bharathiyar Institute of Engineering and Technology, Deviyakurichi. She is currently an Assistant Professor at Selvam College of Technology, Namakkal. Her area of interest is VLSI Technologies.

Govindaraj S received the BE degree in Electronics and Communication Engineering from Anna University-Chennai in 2012. He received the ME degree in Applied Electronics from Anna University-Chennai in 2014.
He is currently an Assistant Professor at Selvam College of Technology, Namakkal. His area of interest is image denoising in medical ultrasound image and image processing.

Selvaraj G received the BE degree in Mechanical Engineering from Anna University-Chennai in 2007. He received the ME degree in Mechatronics from Anna University-Coimbatore in 2009.He is currently an Associate Professor & Head at Selvam College of Technology, Namakkal. His area of interest is VLSI Technologies.