Realisation of 4 To 16 Reversible Decoder Using Verilog

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Abstract: **Reversible logic has become an emerging field for research. The main advantage of reversible logic is power reduction and this advantage have drawn up a significant interest in this field. The aim of the paper is to realize the decoder using Fredkin gate which is basically a reversible gate. There are many reversible logic gates i.e Fredkin gate, Feynman gate, Double Feynman gate, Peres gate, New gate, Toffoli gate and many more. In the reversible logic, reversibility have a special condition which is reversible computing and it is based on the principle of bijection device with a same no of inputs and outputs which means one to one mapping. It finds its application in various fields including quantum computing, optical computing, nanotechnology, computer graphic, cryptography, digital signal processing and many more. Reversible logic is gaining importance in recent years largely due to its property of low power consumption. A comparative study in terms of the number of gates, number of constant inputs, number of garbage outputs and quantum costs is also presented. The circuit has been implemented and simulated in Xilinx.**

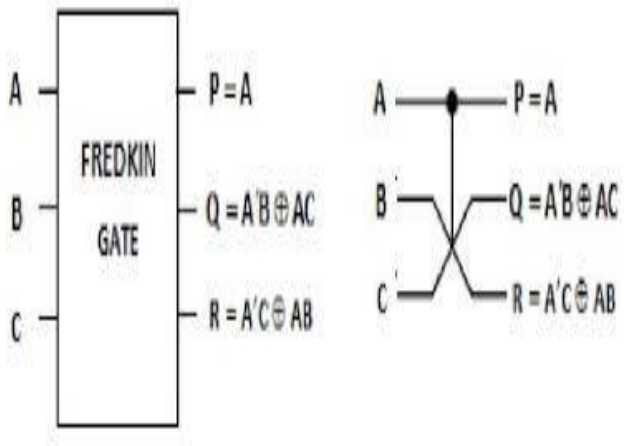
Keywords: **Constant inputs, garbage outputs, reversible gates, quantum cost.**

I. INTRODUCTION

In this era of technology and advancement power consumption has become an important factor of consideration. In this paper we have reduced the power consumption of 4 to 16 decoder by using reversible logic. Reversible logic finds its application in quantum computing, nanotechnology, low power VLSI. In the irreversible logic for the loss of each bit of information [1] proposed that KTlog2 joules of energy is dissipated, where K is Boltzmann's constant and T represents temperature. This amount of heat is very small in simple circuits but it becomes large in complex circuits. Bennett [2] describes that if all the computation is carried out in reversible manner, the power dissipation due to loss of bit can be avoided. Reversible logic involves the use of reversible gates which have same number of inputs and outputs and they can be made to run in backward direction also. Each input in the circuit is associated with some energy. If a bit is lost that is number of bits at the output are less as compared to the inputs ,then energy associated with the corresponding bit is dissipated in the form of heat. Since in reversible circuits no

bit loss is there hence ideally in reversible circuits no power dissipation occurs. But practically some power dissipation do occur, which is much less than the conventional logic. The extra output used in order to make inputs and outputs equal are called garbage outputs. The circuit should be designed in such a manner so as to keep these outputs minimum. However in certain reversible circuits constant inputs are also used. These constant inputs are set either to logic 1 or logic 0 depending upon the operation of the circuit. Reversible gates differ from the conventional logic gates in terms of above two factors.

A. Fredkin Gate: Figure 1 shows the diagram of 3*3 Fredkin gate with A, B, C as inputs and P,Q,R as outputs . Here output "P" is the garbage output that is it is required only for the purpose of obtaining reversibility.



A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

Fig.1 3x3 FREDKIN GATE

It is an n-input n-output logic function in which there is a one-to-one correspondence between the inputs and the outputs. Because of this bijective mapping the input vector can be uniquely determined from the output vector [3]. That is inputs can be calculated with the help of outputs also. Whereas such a feature is not present in conventional logic gates. In conventional logic gates we may have same output for more than one combination of inputs. Various reversible logic gates have been proposed till date, but few of them are described below.

B. Feynman Gate: Let I_v and O_v be the input and output vector of a 2*2 Feynman gate (FG) [4,5] respectively, where I_v= (A,B) and O_v = (P=A, Q=A⊕B). The block diagram for 2*2 Feynman gate is shown in Fig.3.3. (Quantum Cost = 1)

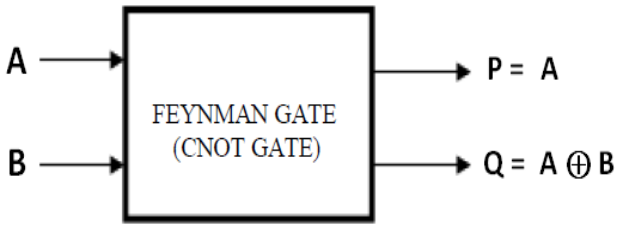


Fig.2 2x2 FEYNMAN GATE (CNOT GATE)

C. Toffoli Gate: Let I_v and O_v be the input and output vector of a 3*3 Toffoli Gate (TG) [6,7] respectively, where I_v =(A, B, C) and O_v=(P=A, Q=B, R=AB⊕ C). Fig.3.7 shows the 3*3 Toffoli gate. (Quantum Cost = 5)

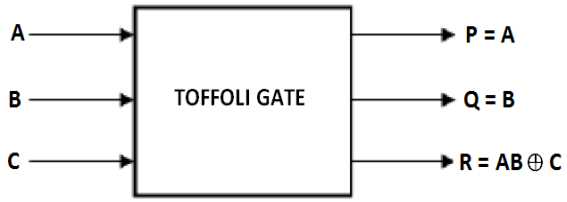


Fig.3 3x3 TOFFOLI GATE

D. Peres Gate: Let I_v and O_v be the input and output vector of a 3*3 Peres Gate [6,8,9] respectively, where I_v=(A,B,C) and O_v=(X=A,Y=A⊕B , Z=AB⊕C). Fig. 3.11 shows the block diagram of 3*3 Peres gate. (Qauntum Cost = 4)

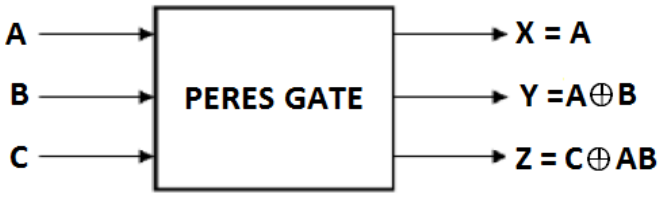


Fig.4 3x3 PERES GATE

Peres Gate is an important gate which has a low quantum cost as compared to other gates. A single Peres gate can give generate and propagate outputs when the third input C = 0. Two Peres gates can be combined to form a full adder.

E. Double Feynman Gate: Let I_v and O_v be the input and output vector of a 3*3 Double Feynman Gate respectively, where I_v = (A, B, C) and O_v = (P=A, Q=A⊕B, R=A⊕C). Fig.3.5 shows the 3*3 Double Feynman gate. (Quantum Cost = 2)

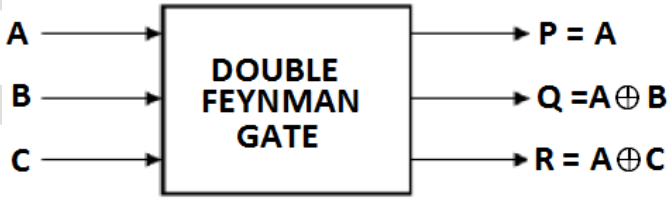


Fig.5 3x3 DOUBLE FEYNMAN GATE

II. CONVENTIONAL DECODER

A decoder is a combinational circuit used in many devices for processing. It has multiple inputs as well as multiple outputs. Generally decoder is available as 2 to 4 decoder, 3 to 8 decoder, 4 to 16 decoder, 4 to 10 decoder. Here a 4 to 16 decoder have been proposed in reversible logic

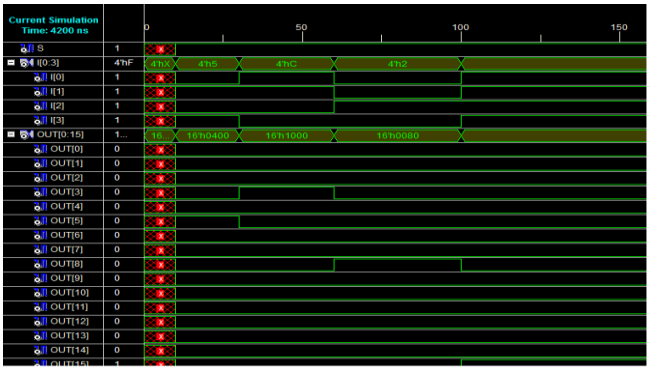
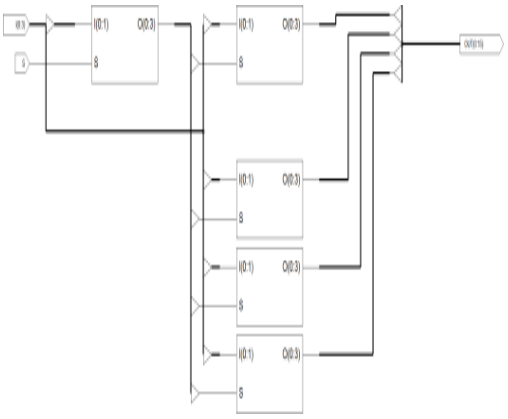


Fig. 6: Conventional 4 to 16 Decoder

III. RTL SCHEMATIC OF 4 TO 16 DECODER



IV. CONCLUSION

In this paper, we have presented a technique to design verilog code for 4 to 16 reversible decoder using Fredkin gate. We have seen that there is a power reduction in the circuit when it is implemented in the reversible logic. Some other reversible gates can be used in design process of reversible decoder apart from fredkin gate. However the circuit consists of 4 inputs,15 constant inputs,10 garbage outputs, 16 outputs. Hence the power dissipation is compared with the irreversible logic gates.

V. ADVANTAGES

What do digital power management and digital heat management even mean?

1. Digital power refers to ordered bit patterns, which can be used to do digital work.
2. Management of digital power involves moving it to where it is needed.
3. Digital heat refers to disordered bit patterns that are no good to anyone.
4. Management of digital heat involves moving it to where it can be dumped.

VI. DISADVANTAGES

1. However, in order to attain the supposed benefits of reversible computation, the reversible machine must *actually* be run backwards to attain its original state. If this is not happening then typically the machine is *heated up* and thus it stops its working.

2. You must make sure weather your computation was performed with no errors when reversible machine actually be run backwards - otherwise chaos (and not the original starting condition) may result when the machine is run backwards.

So: do you think is the reversible logic a waste of time? No. Reversible logic is of substantial significance.

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