Design & Simulation of Single Phase PWM Rectifier with IEEE 519 Compliance

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***Abstract*—In motor drive application rectifier used as an front converter module.Harmonicsinjected in the utility by nonlinear loads, cause major problems that tend to deteriorate the power quality at the mains. In power electronic systems, diode and thyristor rectifiers are commonly applied in the front-end of dc-link power converters as an interface with the grid. Therefore it is required to maintain the power quality. The technique develop the front end converter presented in this paper involves study and implementation of Vector oriented control based converter integrated with four switches to have unity power factor, reactive power compensation, DC link balancing also to have regenerating capability.The proposed method conforms reliability &efficiency operation of single phase front end converter.**

***Index Terms*--PWM Rectifier, vector control, power factor correction, DC link balancing, power quality.**

I. INTRODUCTION

Single phase AC to DC converter is often used to obtain DCsupply from single phase AC mains. The rectifiers are nonlinear in nature and consequently, generate harmonic currents in the AC line power. Issues related to generation of harmonics current by AC-DC single phase rectifier-capacitor filter circuit when connected to the utility network, the legal obligations set forth by the IEEE for limiting generation of low frequency harmonics [1] and different active front end techniques and strategies useful for meeting this standard are studied. To satisfy IEEE 519-1992 power quality standard in converter, are presented. The high harmonic content of the line current and the resulting low power factor of the load cause a number of problems such as voltage distortion and electromagnetic interface (EMI) affecting other users (at PCC) of the power system and increasing volt-ampere ratings of the power system equipment's [2] like generators, transformers, transmission lines, etc.Typical applications of it are UPS, battery chargers and motor drives etc. In most of the applications it is connected at front/utility end of the supply, so that's why it is called as front end converter. The use of single phase diode/thyristor bridge rectifiers as front end converter lead to degradation in power quality due to input current distortion caused by them [3]. The inputcurrent distortion caused by diode/thyristor bridge rectifiers can be reduced by using a bulk input filter, but sometimes it is also required to have a converter with bi-directional power flow capability. In such application the attractive solution is a single phase (Pulse Width Modulation) PWM AC to DC converter.

II. SYSTEM DESCRIPTION

The term Active Front End Converter (AFC) refers to the power converter systemconsisting of the line-side converter with an active switch such as IGBTs, the dc-linkcapacitor, and the load. The line side converter normally functions as a rectifier.But, during regeneration it can also be operated as an inverter, feeding powerback tothe line. Using Pulse Width Modulation (PWM) technique rectifier, active switchingtook places. At input side input rectifier works like boosting chopper will alternatingvoltage. Line - side rectifier is well known as a PWM converter, essential condition is level of peak supply DC link intermediate voltageshouldbe higher. Due to insufficient DC line converter might got saturated to avoid it. Irrespective of rectification & invertionoperation DC link ripple voltage can be resolvedby adequate design of capacitor bank size required. The AFC topology for any typeof load operation.The arrangement of choke for the line - side converter can be between the utility & theconverter. The purpose of inductor is to boost the voltage of converter.Transformersecondary impedance also satisfying the same. For gridmaintained voltage level lineside converter, IGBTs and switched to produced direct current voltage.The line - side voltages generated such a way which control the line currents to therequired value. When DC link voltage drops below fromreference set value,feed-back diodes would carry thecapacitorcharging currents andhelps to bring theDC-link back to reference value.

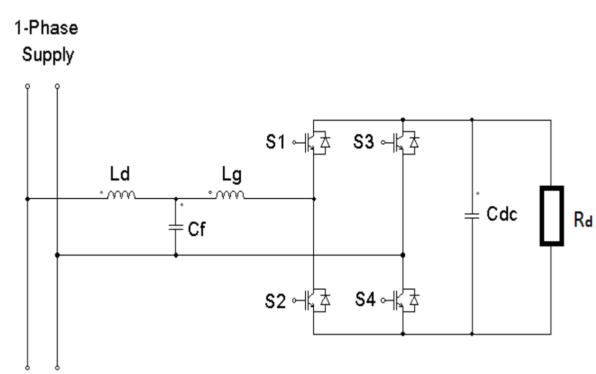
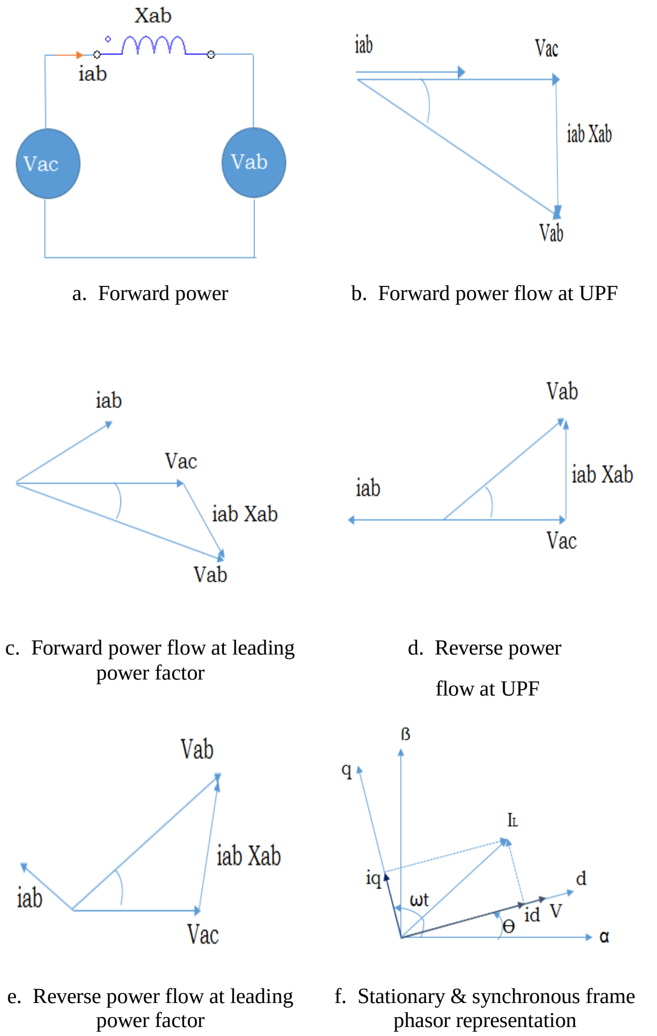


Fig. 1. Proposed Single-Phase Front-End Converter

III. PRINCIPLE OF OPERATION



a. Forward power

b. Forward power flow at UPF

c. Forward power flow at leading power factor

d. Reverse power flow at UPF

e. Reverse power flow at leading power factor

f. Stationary & synchronous frame phasor representation

Fig.2Principle of operation

In the above figure Vacindicates AC grid voltage and Vabindicates voltage at the midpoint of a leg or pole voltage which is PWM in nature. The pole voltageconsists of a fundamentalcomponent at line frequency and harmonic componentsaround the switching frequency of the converter. These harmoniccomponents canbe easily filtered out by choosing proper lineinductance. As we know that activepower flows from leading voltage to the lagging voltage, and reactive power flowsfrom higher voltage to the lower voltage. So both active power andreactive powercan be controlled by controlling thefundamental component of the converter poles voltage withrespect to the grid voltage. That is by controlling the polevoltage w.r.tgrid voltage the currents flowing from the grid can be controlled at any desired powerfactor as shown in above fig.3.

The objectives of the vector control are given as,

- → Voltage regulation of the DC-bus
- → Independent active and reactive power control
- → Bidirectional power flow
- → Operation at any desired power factor
- → Low current harmonics

Vector control of AFC in stationary reference frame: Basically in vector control we have 3 loops

1. Outer DC bus loop
2. Inner active current control loop
3. Inner reactive current control loop

Work with vector control in this project are in synchronous reference frame which can control current as DC quantities, so using PI-current controllers almost zero steady state error can be ensured. As load increases DC-bus voltage reduces that will be sensed and feedback to DC bus voltage controller which increases the current reference so that active current drawn from the supply increases to maintain active power balance between DC-bus side and grid side. Similarly if load decreases DC-bus voltage increases, will give this information to DC-bus voltage controller which reduces the active current drawn from the supply to maintain active power flow balance between DC side and grid side.

IV. BLOCK DIAGRAM AND CONTROL STRATEGY

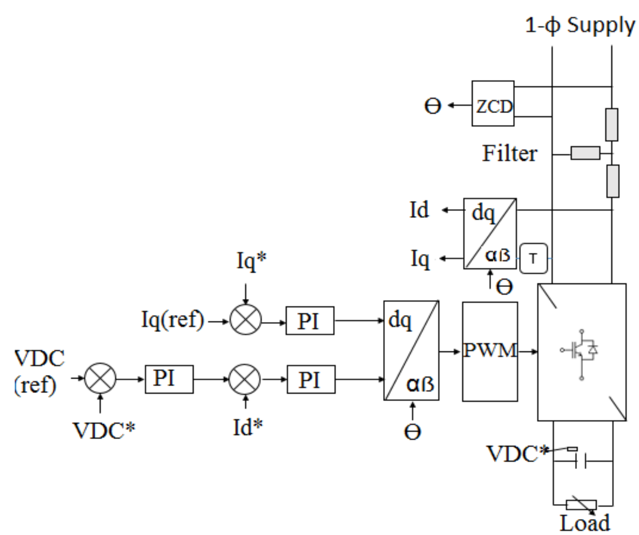


Fig. 3. Block Diagram Proposed Converter

Unity power factor operation if we make reactive current reference equal to zero in inner reactive current loop then we get unity power factor operation. Drawing nearly sinusoidal current by switching the AFC at higher frequencies lower order harmonics get converted to switching harmonics which can be easily eliminated by proper design of high frequency ripple filter.

V. CONTROL ALGORITHM

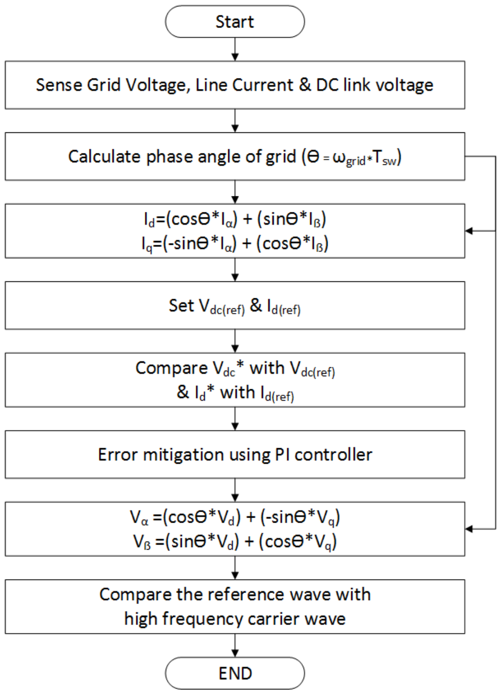


Fig. 4. Block Diagram Proposed Converter

VI. DESIGN OF POWER COMPONENTS

TABLE I

SINGLE PHASE AFC SPECIFICATIONS

Supply Voltage	440V
Supply Frequency	50Hz
Voltage Tolerance	±10%
Frequency Tolerance	±5%
Control Method	Vector Control
Switching Scheme	SPWM Method
Switching Frequency	4 kHz
P.F. Improvement	Yes
Supply Voltage Range	440V ~ 480V
Output Voltage Range	Supply × 1.4142

Design of grid & decoupling inductor: - Grid inductor means inductor in LCL filter normally connected opposite side of the grid (source). And decoupling choke means the inductor connected opposite side of grid inductor. LCL filter is better over L filter, in the case only L filter is connected then it will smooth out the current through the filter. Whereas LCL filter gives harmonics suppression depending upon the design resonant frequency. Harmonics means the (non-fundamental) component in the line current but multiple of fundamental component of current frequency are called harmonics. Lower order harmonics are very crucial to reduce from the line current. For compensation of lower order UPWM Switching scheme has applied and due to that high frequency switching pole voltage will have harmonics at switching frequency. Due to higher switching frequency, high frequency switching ripple takes place in pole voltage as well as in line current that can be reduced by means of LCL filter. Switching frequency is taken 4 KHZ & for that filter designed for 1950 HZ. Decoupling choke is for smoothing of current, also reduce the effects of high frequency switching of IGBT's over PCC current and voltage.

Specification:

Power rating = 55 KVA

Rated current = 150 Ampere

Supply voltage = 440~480 Volts

Frequency = 50 Hz

By taking 12% impedance

$$Z = \omega * L$$

From total inductance grid & decoupling inductance selected ratio 17 & 83 percentage respectively.

High frequency ripple capacitor: - The selection of thecapacitor is a trade-off between reactive power in C andL inductance. The more capacitance, the more reactive power lowing in to the capacitor, and the more current demand fromthe L and the switches. As a result, the efficiency will be lower. The capacitance cannot be too small either. Otherwise, the inductance will be larger in order to meet the attenuationrequirements. The larger inductance L result from smaller capacitance leads to higher voltage drop across the inductor L. The resonance frequency of the filter should be higher than 10 times the grid frequency and then half of the switching frequency. Capacitor used of 51µF, 8A, AC film-capacitor.

$$Cf = \frac{L(g) + L(d)}{L(g) * L(d) * (F * \pi)^2}$$

High frequency ripple resistor: - To protect the H.F. ripplecapacitor from the resonance, damping resistor will be used.Generally the damping resistor value varies from 0.5 ohm to 1ohm. But in 55KVA system the losses in this resistor &heat reduced due to that is critical for us to reduce the loss 0.5ohm will be used. Due to reduced value resistance the voltagespike across the capacitor will be goes up to voltages during the step voltage charge condition. But the capacitor selected is rated 440 Vac peak. Finally wire wound resistor 0.5 ohm, 32 watt is selected for I (resistor) = 8 ampere.

High frequency filter inductor: - To reduce the wattageburden of H.F. ripple filter resistor during the frequencybelow the resonance frequency we are using the inductor in parallelwith theresistor. At resonance frequency the value of inductor is 25.74uh, 5A. Thefollowing is the current waveform passingthrough H.F. ripple filter inductor.Inductor = 4.35 Ampere.

The bode plot of the high frequency ripple filter is shown inFig. 4.The positive peak of the gain at the resonance frequency 1.95 kHz (12.3 x 10^4 rad per second) in the undamped LCL system has been damped by about 98%. Additionally, the increased gain in the low frequency range (below resonance)shows good control feature in terms of command following and low-frequency disturbance rejection. Further, the noticeable change in phase in the low frequency range (below resonance) indicates highly damped gains around the resonance frequency and guarantees the closed loop system stability. It can be further noticed that there is no change in gain or phase at higher frequencies above resonance, which maintains the attenuation performance to avoid the higher order harmonics from being injected into the line by the converter.

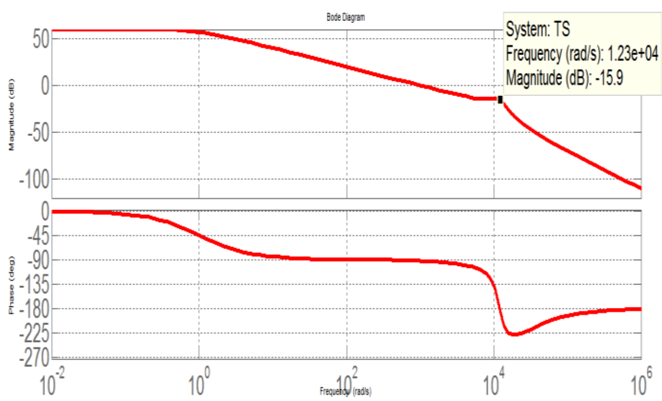


Fig. 5.Bode Plot of LCL Filter Resonance frequency operation

Design of DC link capacitor:-

$$\text{Cdc} = \frac{\text{P(dc)}}{2 * \omega * \text{V(dc)} * \Delta\text{V}}$$

Where P (dc) is Output Power, V (dc) is Output Voltage, ΔV is Voltage Ripple, ω is Angular Speed in rad/sec, Cdcis DC link capacitor required to maintain voltage ripple below three percent.

VII. SIMULATION AND RESULTS

A time & frequency domain simulation of the circuit shown and previously described was carried out in the PSIMenvironment. The total simulation time was 2seconds and the transient load was switched in at 1 seconds. The simulationcircuit parameters areshown in Table II.

TABLE II

SIMULATED PARAMETERS

Circuit Parameters	Range
Grid choke	778 µH
Decoupling choke	156 µH
Filter capacitor	51 µF
Supply voltage	440 V
Grid frequency	50 Hz
Damping resistor	0.5 Ω
Damping inductor	39.78 µH
DC link capacitor	7.05 mF
IGBT rating	450 A / 1200 V

Here, the input has been taken from AC mains, this single phase is converter with the help of park transformations. One of these two phases is been compared with the desired output level, that gives error signal. Now, with the help of inverse park transformation the generated error signal is again converted to phases. This obtained single phase is now compared with the triangular waveform to obtain the pulses. These pulses are then given to the Active Front-End Rectifier as an input to produce the desired output power. This is narrated by the block diagram Figure 2.The performance ofthe proposed control strategy and thefront-end convertertopology has been verifiedby the simulation results obtained with the help of PSIMsoftware. The mains phase voltage istaken as 440V rms witha supply frequency of 50Hz. Thecapacitance of the DC linkcapacitor is taken as 4700µF each and the boost inductanceconnected in line is taken as 934µH.A switching frequencyof 4 kHz is chosen. A passive switchingload of 7.04 Ω andother load are taken. The twoloads here show therated-load and transient-load conditionsfor the converter. Thedesired DC link is set at 700V which is appearing across thecapacitor. The simulated waveforms for the phase voltagesand the line currents of the converter in the rectification modeare shown in Figure.5. The harmonicspectrum of the inputline current is shown in the Figure.6. It has a % THD of only2.55 % which is within prescribed harmonic standards. This isa highly desirable feature of a high power factor converter.Figure.7 depicts the waveforms of the load voltage and theload current in the rectification mode. The converter nowundergoes the sudden change of load and thechange in the dc output waveform and the line currents isshown in the Figure.8. The converter still retains the samedesired DC output and the current THD becomes ≤2.55% and maintaining power factor unity as shown in Figure.9. The DC output ripple in any case ofloadingremains within the limit at 700 V. Thus the proposed control strategy of the limit of ± 14V. The input powerfactor during both the cases remains close to unity. During both the cases the DC linkacross the capacitor remains balanced, theDC link is converter maintains the DCbus capacitor voltages under all the conditions of load andalso improves the power quality.

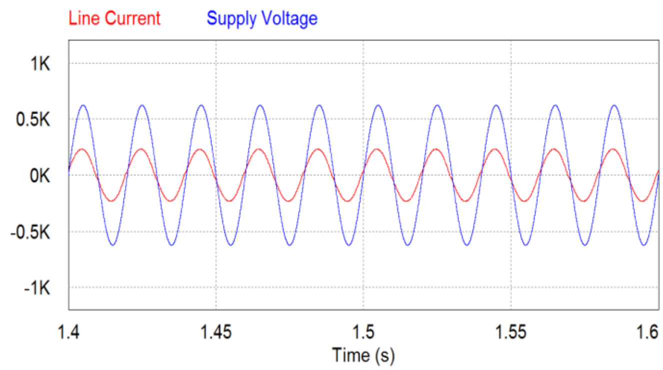


Fig. 6. Waveforms of Phase voltage and line current

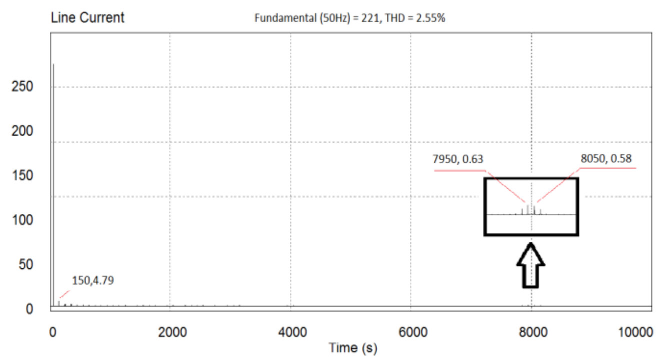


Fig. 7. Harmonic Spectrum of Line current

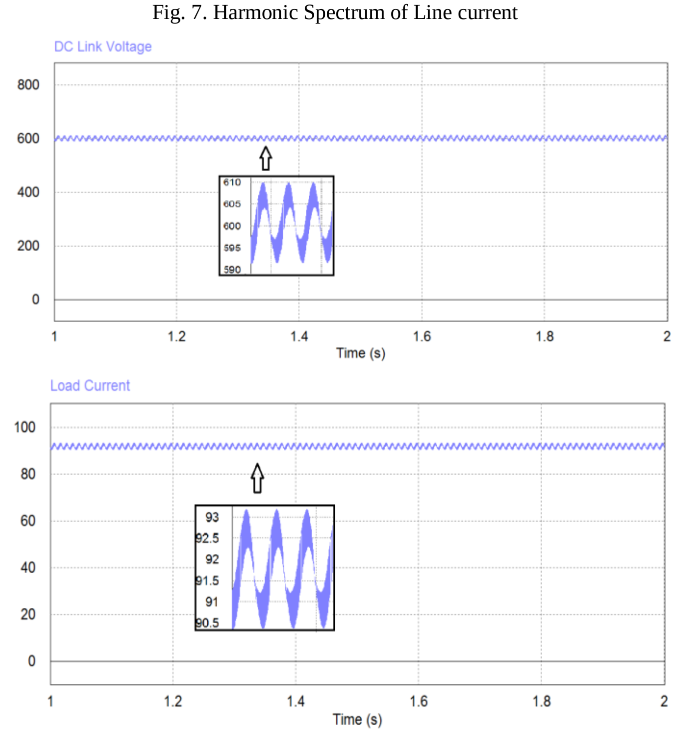


Fig. 8. Load Voltage and Load Current

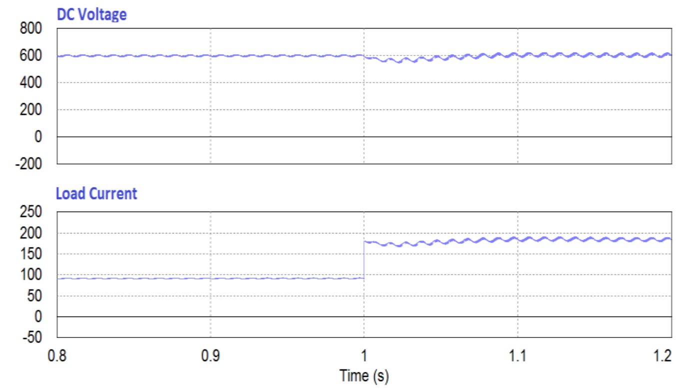


Fig. 9. Waveforms of DC Link at load change
(After 1 sec load changes)

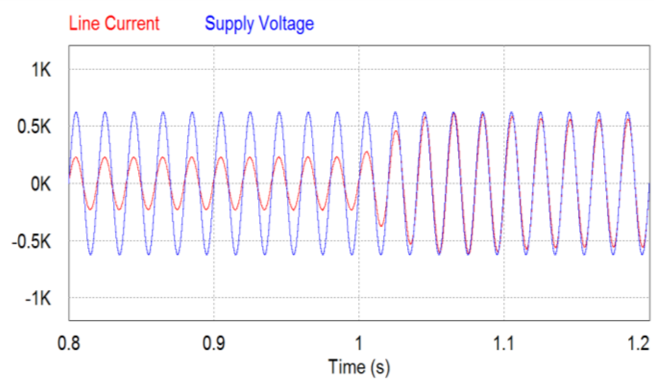


Fig. 10. Waveforms of Phase voltage & Line current at load change
(After 1 sec load changes)

TABLE III

LOAD REGULATION

Load (%)	V_{in}(V)	I_{an}(A)	V_o(V)	I_O(A)	(I/P)PF	%THD_i
100	415	140.67	600	91.66	0.99	2.740
75	415	103.39	600	68.75	0.99	3.335
50	415	68.88	600	45.83	0.99	4.953
25	415	34.90	600	22.91	0.98	5.913

VIII. CONCLUSION

In this paper, single-phase front-end converter is proposedto achieveunity power factor at input side with limiting line current harmonics, well regulated and balanced DC link voltage at theoutput with capacitor voltage balancing, regeneration capability and also reactive power compensationusing voltage oriented control. The proposed controlstrategy was based on sinusoidal pulse width modulationtechnique for switching. The converter does not allowthe harmonics and reactivepower to flow in the system.Balancing of DC link is achieved by voltage oriented control technique and line current harmonics filtering is by means of high frequency ripple filter.

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