Full Adders using Quantum Dot Cellular Automata (QCA)

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***Abstract* – The advancement in technology is one thing the world always looks forward to. From vacuum tubes to the CMOS transistors, the technology has evolved at an exceptional rate. CMOS is the best one could have given for semiconductor industry but, the question is "What's next?". Quantum dot Cellular Automata is one of the answers for the next technology after CMOS. QCA is an ongoing research technology which is expected to have very bright future. The problems which are present in current CMOS technology are addressed by the QCA technology effectively. It offers better area, power consumption, operational speeds compared to CMOS technology. The problems due to power dissipations can be solved by using Reversible technology. It is an emerging and one of the compatible technologies along with the QCA. In this paper, two Full adders in both reversible and irreversible logics are discussed and compared.**

***Key Words*: QCA, Full Adders, Reversible logic, Irreversible logic, Low Area, Nanotechnology.**

I. INTRODUCTION

The Moore's law states that, number of transistor in an area doubles for every two year. But doubling the number of transistor leads to shortening of gate length which causes anomalies in its working and also reducing the transistor causes higher power dissipation in the circuits. To solve these complications, new emerging technologies like QCA and reversible logic are considered as suitable replacement for CMOS technology. The International Technology for Semiconductors (ITRS) reported that the current CMOS technology would not survive after 2019 due to the listed complications [1], [2].QCA was introduced by C.S. Lent et al. in 1993. QCA was promising is increasing the switching speeds of the circuit as the information was passed using electrons unlike CMOS technology where information is transferred through current or voltage [3]. QCA is expected to have higher density of circuits and lower power dissipation compared to CMOS. In this paper, QCA technology is used to develop low power, high device density adder to nanoscale circuits.

II. BASICS OF QCA

2.1 QCA Cell

QCA cell is the fundamental block of the QCA technology, QCA cell consists of four holes at each corner of the cell. Each QCA cell has two electrons which are present at opposite sides of the cell diagonally due to columbic forces of repulsion. Due to two polarization states, logic "0" and logic "1" displayed in Fig. 1. In QCA technology, information is propagated by cell polarization states, as state of one cell can be strongly influenced by neighbouring cell.

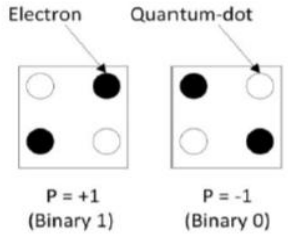

Fig.[1] . QCA Cell

2.2 QCA Wire

When the QCA cells are placed in the sequential manner they form the QCA wires. The signal can be transmitted from one cell to the other cell through the wire. It uses columbic principle of repulsion to transmit the data. These QCA wires are more suited for binary data transmission. QCA wires are classified based on the polarization of the QCA cell. A 90° aligned QCA wire is one where polarization of input cell is once fired will other cells in wire as demonstrated in Fig. 2, whereas 45° aligned QCA wire also known as anti-align QCA wire shows negation property [5] as displayed in Fig. 3. Thus the output of wire is the negation of input as cells in a wire are 45° rotated.

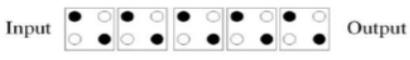

Fig.[2]. QCA Wire 90°

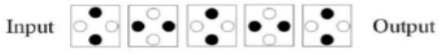

Fig.[3]. QCA Wire 45°

2.3 QCA Crossover

In QCA, wire crossing can be done in two methods, Single layer (Coplanar layer) and a multilayer crossover. Coplanar layer crossing the whole design is in the same layer and the crossing is done via 90° and 45° QCA wire as displayed in the Fig. 4.

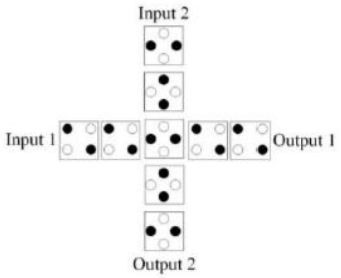

Fig.[4]. Coplanar Crossing

In a multilayer crossing, we use more than one plane to perform the wire crossing as shown in Fig [5].

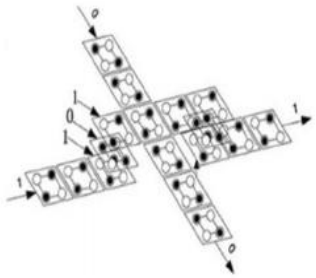

Fig.[5]. Multilayer Crossing

2.3 QCA Clocking

QCA clock is the most prominent factor in QCA based designed circuits. QCA Clock not only delivers power to the circuit but also control the direction of data flow. In QCA clock cycle is consist of four phases. The four phases are switch, hold, and release and relax as depicted in Fig. 6. Normally, a cell is in un polarised state. Cells get polarized during the switch phase and act as a latch during the hold phase and un polarised during relax and release phases [6].

III. PROPOSED WORK

In this paper, we are presenting a simple circuit to realize the full adder using both Reversible and Irreversible logic with minimum number of cells.

3.1 Irreversible Full Adder

The Full adder is realised using a 5- input majority gate and a 3- input majority gate. It is the simplest approach for a full adder and it uses 38 QCA cells and offers no clocking delay. The Full adder and its results are given in Fig.[7] and Fig.[8] respectively.

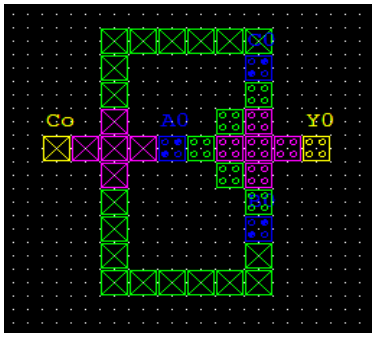

Fig.[7]. QCA Proposed Layout

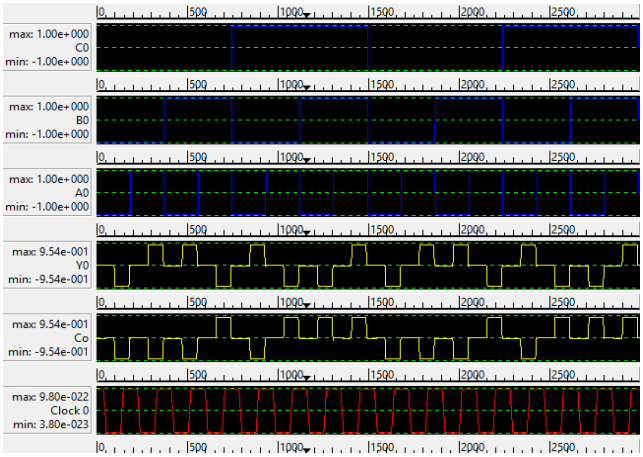

Fig .[8]. QCA Output waveform

3.2 Reversible Full Adder

The Full adder is realized using the Peres Gates as the building blocks. Peres Gate is a 2- input and a 3- output reversible gate and its functionality is explained in Fig.[9] and its layout and results are shown in Fig.[10] and Fig.[11] respectively.

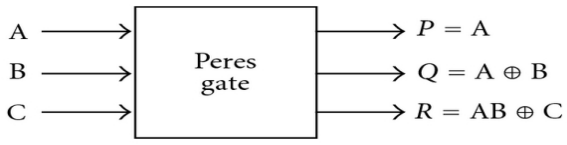

Fig.[9] Peres Gate

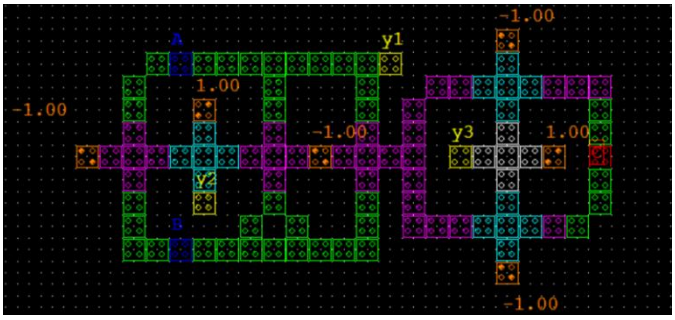

Fig.[10] Peres Gate Layout

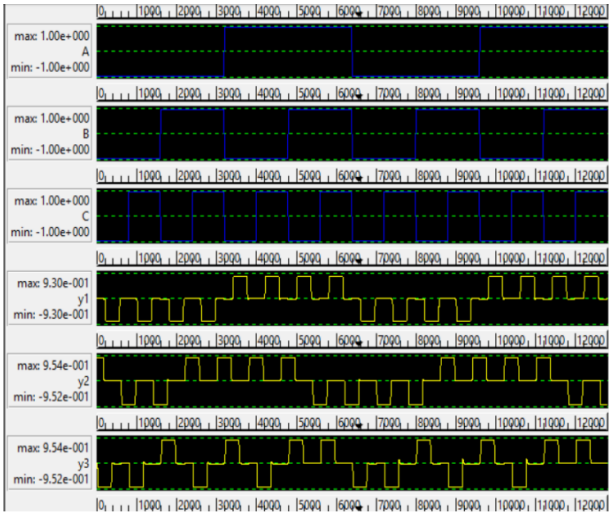

Fig.[11] Peres Gate Output Waveform

The Full adder is realized using two Peres gate and the output is generated as shown in Fig.[12] and Fig.[14] respectively.

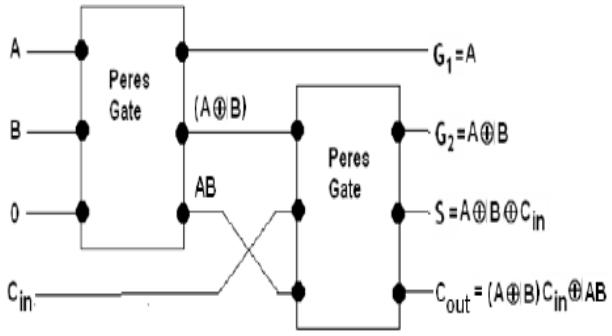

Fig.[12] Full adders using Peres Gate

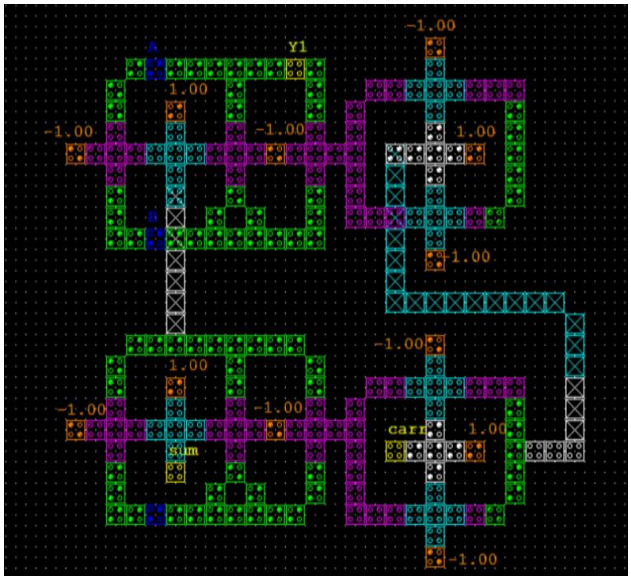

Fig.[13] Reversible Full adder

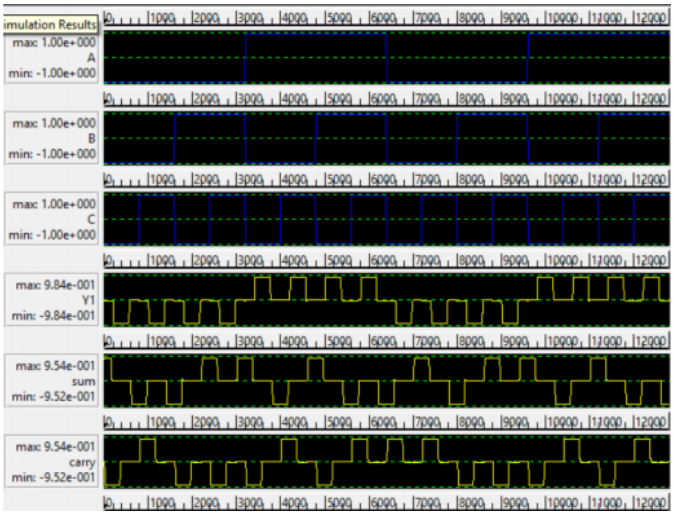

Fig.[14] Reversible Full adder output waveform

Table -1: Comparing Reversible and Irreversible Full adders

Approach	*Area*	*Delay (clk)*	*No. of cells*
Irreversible	0.04μm^2	0	38
Reversible	0.14 μm^2	2	224

IV. CONCLUSIONS

In this paper, the basics of QCA are discussed and it explains how this technology can help to design and develop low power circuits. The focus of this paper was on efficient design of a Full adder circuits using minimum number of cells in both Reversible and Irreversible logics. The two adders can be compared and offer good results and irreversible full adder offers a simple approach but the reversible full adder offers a much complex approach and offers more delay. These adders can be further used to design and develop multi bit adders and multiplier circuits.

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