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Modern Implementation of Image Processing Algorithms on FPGA

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ABSTRACT

Field-programmable gate arrays (FPGAS) have emerged as a powerful platform for real-time image processing due to their inherent parallelism and configurability. This paper presents an optimized hardware implementation of fundamental image processing algorithms including Sobel edge detection, Thresholding contrast stretching and negative transformation using VHDL on FPGA architecture. Unlike conventional CPU and GPU-based systems, which rely on sequential execution, the proposed design exploits spatial and temporal parallelism to achieve high throughput and low latency.

pipelined architecture combined with line buffering and window-based processing is adapted to efficiently process streaming pixel data. The system is validated using modalism simulation and Mat lab-based verification. Experimental results demonstrate that the FPGA implementation processes a 256×256 image frame in 0.019 seconds at a 10 MHZ clock frequency achieving approximately 10×–13× speed improvement over Mat lab-based software execution. The proposed architecture also ensures efficient resource utilization and is scalable for real-time applications such as surveillance, object detection and embedded vision systems. the results confirm that FPGA-based implementations provide a viable solution for high-performance, low-power image processing and industrial Robots, 5G Networks And AI Inference Applications.

Keywords— FPGA, VLSI and Enhancement, pipeline

INTRODUCTION

IGITAL image processing focuses on the manipulation and analysis of images using computational algorithms to enhance visual quality, extract meaningful information, support automated decision-making. Traditional software-based approaches process image pixels sequentially, which limits their performance in real-time applications. In contrast, Field Programmable Gate Arrays (FPGAs) provide a hardware-based solution that enables Parallel processing, significantly improving computational speed and efficiency. Unlike Application-Specific Integrated Circuits (ASICs),FPGAs can reprogrammed and reduced development cost. FPGAs are reconfigurable devices composed of logic elements and memory blocks and programmable interconnections highly suitable for high-throughput image processing tasks. In FPGA-based systems, images are processed as continuous pixel streams rather than complete frames, reducing latency and memory requirements.

Neighborhood-based operations, such as filtering and edge detection, are implemented using windowing techniques and line buffers stored in on-chip memory. A wide range of image processing algorithms including enhancement filtering, edge detection and geometric transformations, can be efficiently implemented on FPGAs, hardware description using languages such as Verilog or VHDL, simulation, synthesis, and verification. FPGA-based image processing systems are widely used in applications such as video surveillance, medical imaging, and computer vision. Traditional software handles pixels one after another, but FPGAs process them using parallel pipelines. FPGAs can do several tasks at once, such as handling different pixels or steps in an image processing pipeline simultaneously.

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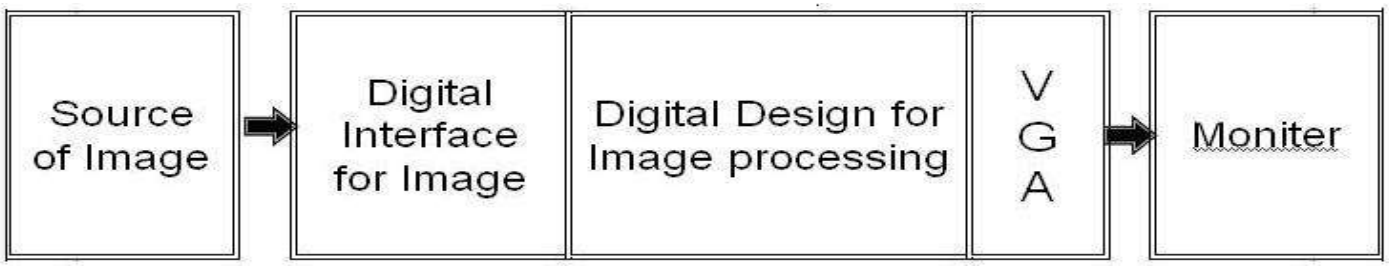

Fig. 1. Block Diagram of Image Processing

This setup allows a new pixel to be started every clock cycle. For operations like convolution or filtering (such as Sobel and Median filters) a small part of the image (like a 3x3 or 5x5 window) is held in a special memory area (on-chip RAM) so that it can be used repeatedly without needing to store the whole image. adaptive automation and deep learning to handle messy images and complex scenes. Filtering Gaussian Blur and Median, Mean, Smoothing Removing unwanted noise or preparing images for further processing. Edge Detection Sobel and Canny, Prewitt, Robert Identifying the edges or boundaries of objects in an image. Morphological Erosion, Dilation Changing the shape of objects in binary images. Transformations Gray-scale conversion The "Modern" Aspect Shift from RTL to HLS Mention that modern implementation has moved from tedious Verilog/VHDL coding to High-Level Synthesis(HLS).Logic Design, Logic gates, FSM(Finite State Machines),Timing analysis. Simple enhancement (Negative transformation) start to complex (CLAHE, Edge Detection) work it. You can change the logic even after the hardware is built. Highlight that FPGAs provide high performance-per-watt compared to power-hungry GPUs.

A. Algorithm Focus

Clearly state which algorithms you are implementing (e.g. Sobel Edge Detection, Gaussian Blurring or Median Filtering).On Zynq boards AXI interfaces or DMA (Direct Memory Access) use data transfer speed increase. Images convert Hexadecimal or Binary format(using MATLAB/Python) because FPGAs directly image files not read. Vivado Simulator design verify it.

B. CPU/GPU Limitations

Explain that traditional software (C++, Python and MATLAB) running on General Purpose Processors (CPUs) is sequential.

C. Latency Issues*:* Software-based processing often struggles with "Real-time" requirements because it handles pixels one by one, leading to delays (latency) and high power consumption.

D. System-on-Chip

Mention platforms like Xilinx Zynq which combine an ARM processor with FPGA logic for smarter processing.

E. Line Buffering

To access a 3x3 neighborhood in a stream, FPGAs use line buffers (on-chip Block RAM) to store previous lines, allowing access to vertically adjacent pixels at the same time.

F. Pipelining:

Complex algorithms are broken into smaller parts, allowing a new pixel to enter the process every clock cycle before the previous one is done. Algorithm Use case Point Processing Brightness/Contrast adjustment, Inversion, Basic image improvement.

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G. Matching

Advanced SIFT algorithms now run at 33 milliseconds per image for 2K resolution, which helps robots and aerospace systems track features in real time. Neighborhood Filtering Median filter, Sobel edge detection, Gaussian blur Noise removal and feature extraction. Geometric Transformations Scaling, rotation and warping Image correction and perspective adjustment. Complex Analysis Object tracking, Convolutional Neural Networks (CNNs) Advanced computer vision and AI applications. The PC is the source of the image, which sends the image to the digital hardware (FPGA). The image is sent to the digital hardware using the Transport utility of the Diligent board.

The gray values of the image received from the PC are Processed by the digital hardware designed on the FPGA reconfigurable computing technology well-suited for video processing. FPGAs self-working "vision-on-a-chip "systems. Vision Transformers (ViTs) and making it easier to deploy these systems with HLS. The digital hardware includes designs for various spatial domain image enhancement techniques such as negative image, threshold and contrast stretching etc. Modern FPGAs have enough logic resources to handle even complex tasks on a single chip. These systems can also change their setup depending on the environment they're working in. This makes FPGA-based systems naturally flexible. VGA was the first graphical standard adopted by most manufacturers. Tools like FFVTA use one design to handle the tricky self-attention part of Transformers making them faster by up to 16.6 times on devices like the Xilinx Kria KV260.

FPGAs are now vital for real-time diagnosis, such as detecting skin cancer and identifying seizures, with over 99.4% accuracy and very low power use (0.116 microwatts).Aerospace High-resolution vision systems have been made safe for space using radiation-resistant hardware like the Nano Xplore NG-Ultra for long missions.

H. Problem Statement

Traditional software-based image processing systems suffer from high latency and limited real-time performance due to their sequential execution model. These limitations make them unsuitable for high-speed and embedded vision applications.

I. Objectives

To design and implement real-time image processing algorithms on FPGA.

To optimize Sobel edge detection using pipelined architecture.

To compare FPGA performance with MATLAB-based software implementation.

To analyze system latency, throughput, and execution time.

To evaluate hardware efficiency in terms of architectural design.

REVIEW OF LITERATURE

Recent advancements in FPGA-based image processing have demonstrated significant improvements in real-time performance and energy efficiency compared to CPU and GPU-based systems [1], [2]. Researchers have shown that pipelined and parallel architectures enable continuous pixel processing, achieving high throughput with minimal latency [3]. These implementations utilize line buffers and sliding window techniques to efficiently perform convolution operations [4]. Additionally, hardware/software co-design approaches integrating ARM processors with FPGA fabric have gained popularity for balancing flexibility and performance [5]. Recent studies also explore High-Level Synthesis (HLS) tools to accelerate development time while maintaining acceptable performance [6]. However, challenges remain in optimizing resource utilization, power consumption, and scalability for high-resolution image processing.an optimized pipelined architecture for Sobel edge detection and comparing its performance. Digital image processing uses algorithms to improve picture quality and extract useful information. FPGAs are hardware reprogrammed solutions that can process

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multiple pixels at the same time, much faster and more efficient, ASICs is expensive and risky, so FPGAs are often a better choice. Allowing for updates, adding new features, or fixing bugs without replacing the physical chip.FPGAs use parallelism to do high-speed image processing (like over 30 images per second)

A . Resource Sharing

Instead of making duplicate logic, FPGAs reuse existing resources, like using the same processing path for different data parts to reduce signal routing issues. Contrast stretching uses two threshold values, which are provided by the user. Contrast stretching is performed. If the input is less than the threshold, it is stretched toward the darker side by subtracting a constant.

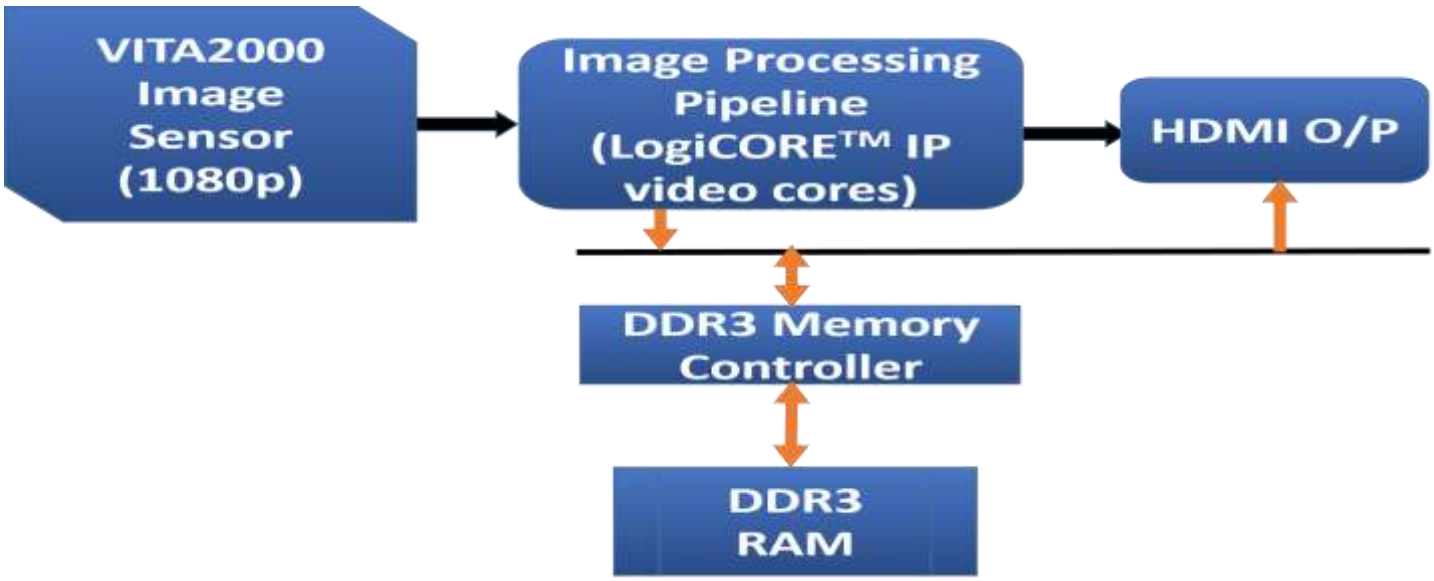

Fig.2. Image Processing Pipeline

If the input is greater than the threshold, it is stretched toward the brighter side. An edge, we only need the magnitude the FPGA system architecture. A buffer is through random access processing. At the same time, the path between input and output buffers is continuous. There's no need to stop and store data randomly. Therefore, stream processing can be used. The next step is to identify the FPGA mapping techniques that can achieve the desired system performance.

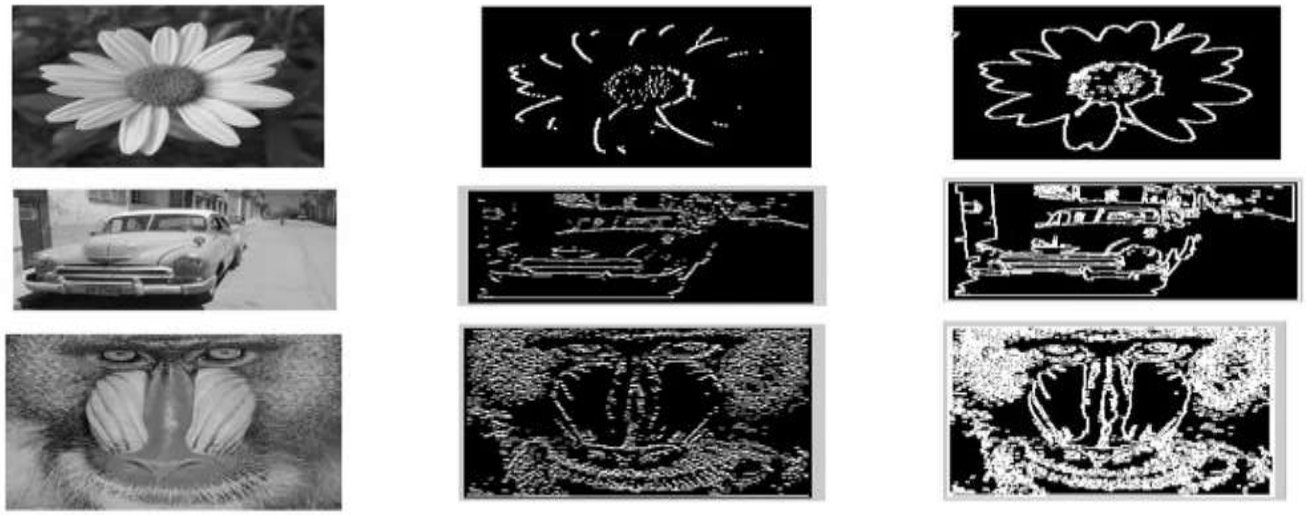

Fig.3 . Image Contras Changing

Edge is a sudden change in brightness. Just like in a one-dimensional signal, a sudden change can be identified as either a peak or a valley. So, to detect this sudden change, since an image is a two-dimensional signal, we

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need to calculate the derivative in both the x and y directions. The resulting derivative image is a vector, which means it has both magnitude and direction.

TABLE I Comparison Of Fpga And Gpu

Feature	**FPGA**	**GPU**
Performance	High, Deterministic	Very High Throughput
Latency	Extremely Low	Moderate/Variable
Power Efficiency/development	High(1.2–22.3x) (Complex)	Low(Easy)
Flexibility	Reprogrammable	Fixed Architecture

B.Transformer-Based Edge Detection (Ranked & Sauge): Special types of loss functions called "ranking-based losses" to find object edges with very high accuracy. three main categories of Algorithms based on how they handle data.

Low-Level: These focus on simple pixel-based tasks like finding edges, smoothing images, and converting image formats.

Intermediate-Level: These deal with processing groups of pixels, such as adjusting contrast and performing shape-related operations like expanding or shrinking images.

High-Level: these are for understanding images, like finding key points and matching features, which used to be done only in software but are now being adapted to work on FPGA hardware. FPGAs in space, testing if standard processing methods can be used on devices like the Nano Xplore NG-Ultra. Many systems use a mix of FPGA and a small processor like Cortex M0 or ARM to keep fast pixel processing and flexible decision-making.

TABLE II Comparison of Modern vs. Traditional Algorithms

Algorithm	Type	Best For	Benefit over Sobel /Threshold
Sam 2	Foundation Model	Complex Scenes	No manual threshold understands”objects."
Adaptive Sobel	Hybrid	Real-time / FPGA	Automatically finds the best threshold.
Bdcn/ Hed	Deep Learning	Artistic / Detailed	Multi-scale detection very low noise.
RBF INTER POLATION	Mathem-atical	Medical X-rays	Extremely precise boundary localized

Pipelining produces one output per clock cycle after a short start-up time, making it great for fast gray scale image processing. Limited resources like DSP slices and BRAM restrict how many steps can be done in parallel.

METHODOLOGY

FPGAs to process images directly on satellites Using 65 nm FPGAs can create very low-power designs, sometimes meeting the performance of custom chips. Using approximate address can Optimizing how memory is used can cut power by up to 30% without affecting performance.

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Architecture FPGAs are great for specific, high-speed tasks, while GPUs are better for general, big-data tasks.

1. Timing Constraints 2.Physical Constraints 3. I/O Standards 4.Resource Constraints

5. Logic Cells/LUTs 6.Memory Blocks (BRAM) 7. DSP Slices 8. Power Constraints

9. Performance & Latency:

A. VHDL/Verilog Implementation

This method involves writing the hardware structure manually, giving the most optimization but at the cost of complexity

Core Architecture: Uses a line buffer to store rows of image data, letting the system take a pixel window for convolution.

Convolution Process: The pixel window is multiplied by two masks (horizontal and vertical) to calculate intensity gradients.

Performance Benefits: Manual coding allows for very precise bit-width optimization and direct control over each clock cycle, often leading to slightly lower resource usage than automated tools.

Challenges: Requires handling complex timing, SD Card, Camera Interface like MIPI CSI-2, or MATLAB-to-FPGA JTAG memory interfaces, creating custom test benches for verification.

Modern Design Flow: High-Level Synthesis Implementation HLS lets developers write algorithms in C or C++, which the tool then turns into VHDL or Verilog.

Rapid Prototyping: Significantly cuts development time often by weeks by hiding low-level hardware details. Productivity Tools Uses libraries like Vitis HLS Video Library or HL Open CV, which have pre-made functions for Sobel filtering and colour conversion.

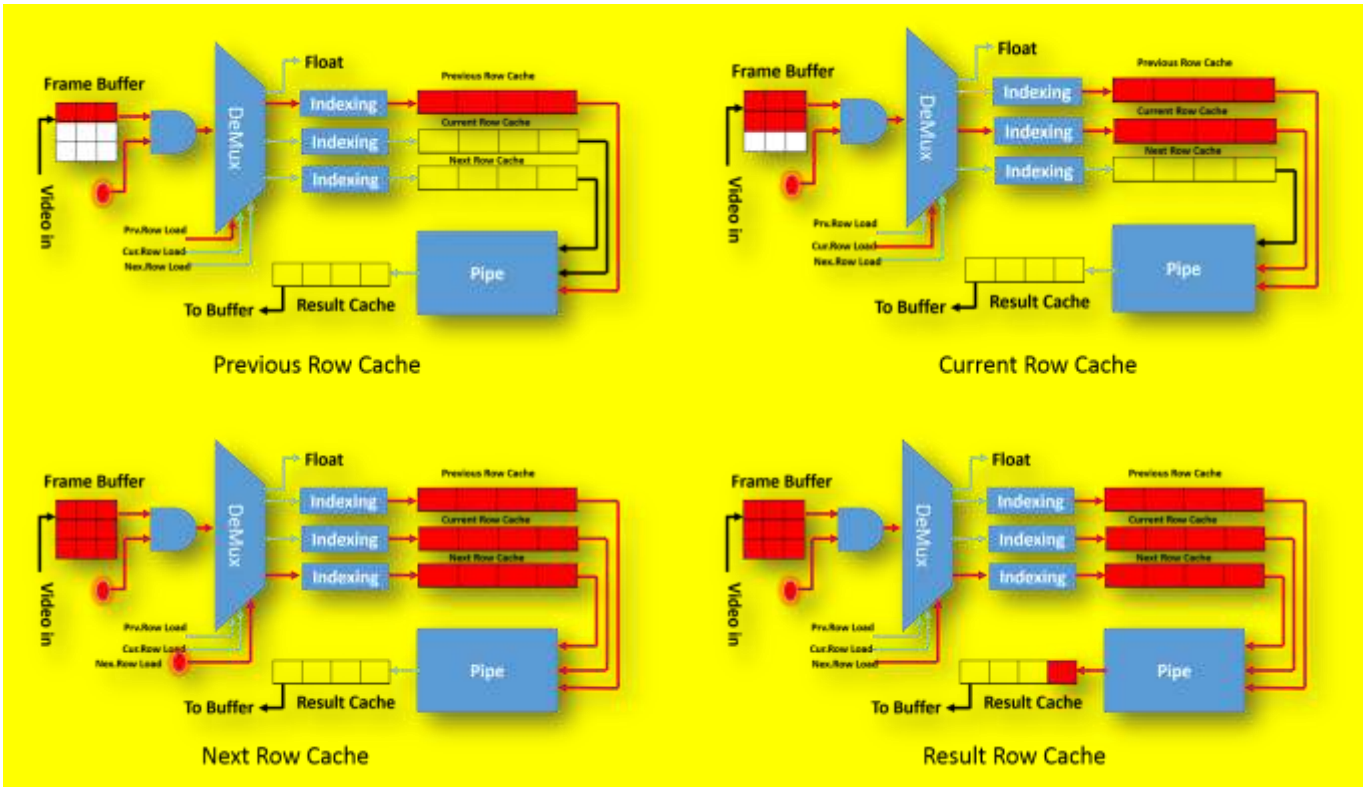

Fig.4. over All Edge Detection System Architecture

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B. Resource Utilization (Luts, Bram, Dsp Slices)

Look-Up Tables (LUTs): LUTs are the main building block of an FPGA, used for making different types of logic and state machines. Modern FPGAs, such as Xilinx 7-series, have 6-input LUTs that can also be used for small memory or shift registers (LUT-SR).

Block RAM (BRAM**):** These are special memory blocks on the chip used for holding large data without using LUTs.

DSP Slices (Digital Signal Processors**):** These are special blocks on the chip made for fast math operations. Designers often choose between using DSP slices or LUTs. If DSP slices are scarce, they may use LUTs but that means slower performance and more space. While performance is very good, HLS may use a bit more FPGA resources (LUTs/Flip-Flops) than a hand-optimized VHDL design.

C. Image Enhancement and Edge Detection Algorithms

Such as Sobel, threshold, and contrast stretching are selected and Sobel mask is implemented in a pipeline. The pipeline has three stages. The derivative pixel is stored in the output cache Memory in the third stage. While the current pixel is being stored in the output cache, the derivative of the next pixel is calculated in the second stage. At the same time, the third pixel is fetched in the first stage. Suppose the incoming frames are 256 × 256 in resolution. If the system needs to process 50 frames/second. The clock speed chosen for this design is 10 MHz because in one cycle, none of the pixels are fully processed. Some parts of the processing are done during In the simulation, output is written to a file, and if the file writing is slow, the data has to wait in a buffer, which increases system delay in the simulation environment. Usually, image intensity values are stored as eight bits. The partial product operation involves multiplying by 2 and then adding. So the maximum integer value that can be produced is (255 x 2 + 255 + 255 = 1020), which needs 10 bits to be represented [3]. If we include one more bit for the sign, the data bus should be at least 11 bits wide.

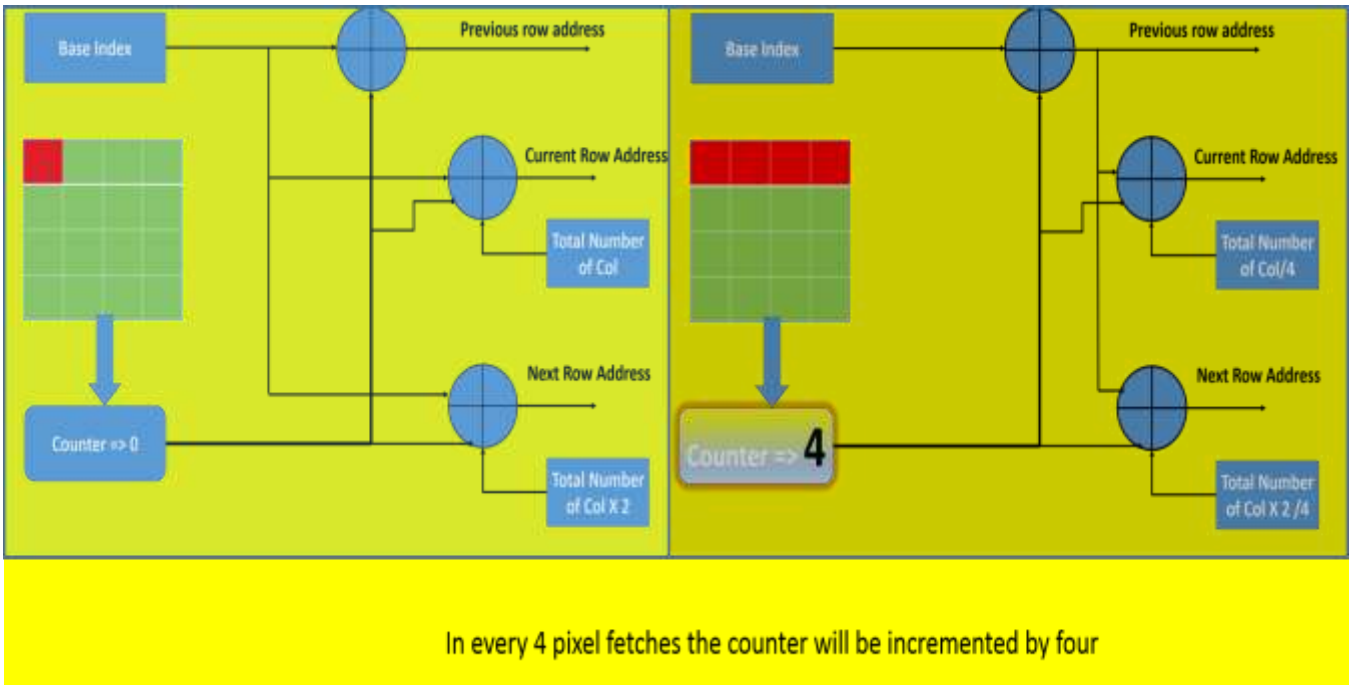

Fig.5. Indexing Circuit

The entire circuit can be divided into four sections the buffering part, indexing part, caching part, and pipeline. Data from the test bench is stored in the internal frame buffer. This data is then sent to cache memory through the right control signals. If eight read operations are done for each result pixel, the system's bandwidth usage

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will be inefficient. Four pixels are fetched at once from the buffer and stored in a 4-byte cache. Four pixels from the previous, current, and next rows are stored in three different cache memories, When the first row of the buffer is full, the test bench sends a horizontal synchronous pulse, which allows the data path between the buffer and the cache for the current row (present row cache).In a similar way, data flows from the buffer to the cache for the current and next rows. Directives & Pragmas The path from the pipeline to the cache for the result pixels is only enabled once the input row caches are full, to avoid junk data at the result cache. When the result cache is full, the 4 bytes are written to the result frame buffer and then sent to the VHDL display module of the test bench. The sequence of events involved in data flow is shown in fig. a red line shows an enabled path, and a green line shows a disabled path. They can process data in multiple places and times at once. Vision FPGA Implementation for Image processing is the new FPGA-Based Soft-Core Processors for Image Processing the "Discussion" phase of FPGA usually looks at how hardware limits and design choices affect performance and use of resources.

Threshold The data flow needs to access eight neighboring rows to calculate the derivative of a single pixel. Because of this, pixels can't be processed immediately since the system has to wait for the needed pixels. The buffer is filled one after another, so the minimum waiting time for the system is the time it takes to get the first three rows from the test bench. Once the third horizontal synchronous pulse is received from the test bench, the data flow to the system starts. For further processing, this data is converted into an unsigned format because of the arithmetic operations involved.

Data Analysis and Interpretation Of Results

The SOBEL mask is used in the pipeline section has 3 × 3 registers. Each register holds three pixels: one from the previous row, one from the current row, and one from the next row. The total size of the internal registers in the pipeline is 12 bytes. The coefficients of the SOBEL masks are stored in another set of register banks. The sums from the convolution process in the 'x' and 'y' directions are calculated at the same time and stored in Dx and Dy registers. In the next clock cycle, the modulus value of these pixels is calculated and stored in the |D| register. This value is written to the result cache in the next clock cycle.So the pipeline has three stages. In the first stage, Dx and Dy are calculated. The second stage calculates the modulus, and the third stage stores the pixels in the result cache. The sequence of data flowing red square blocks represent the pixels, and the red arrows show the enabled paths. At the end of each row of input pixels, the pipeline is flushed. After the flushing, the data path leads to the output cache.

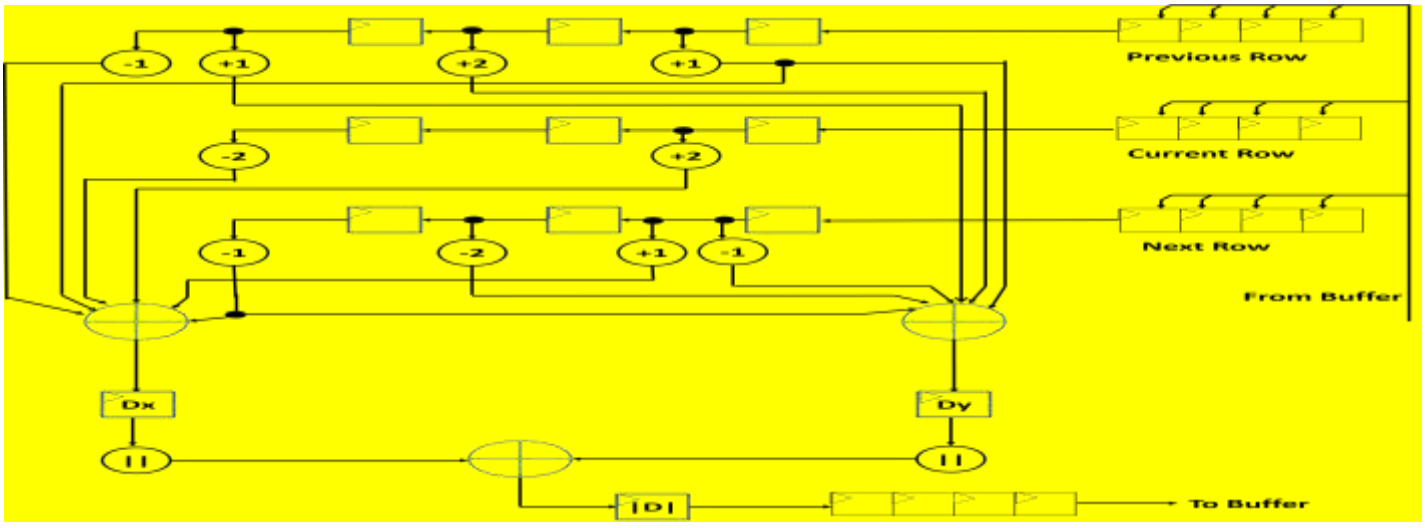

Fig. 6. Pipe-line Circuit

Memory Management & Optimization Memory will stop working for 3 clock pulses. During these 3 clock pulses, data from a new row will be moved into the pipeline. The result INoutput frame buffer. Four pixels from the result cache will be sent to the output frame buffer using indexing circuits. In this module, the output composite signal will be changed into a hex-image file.

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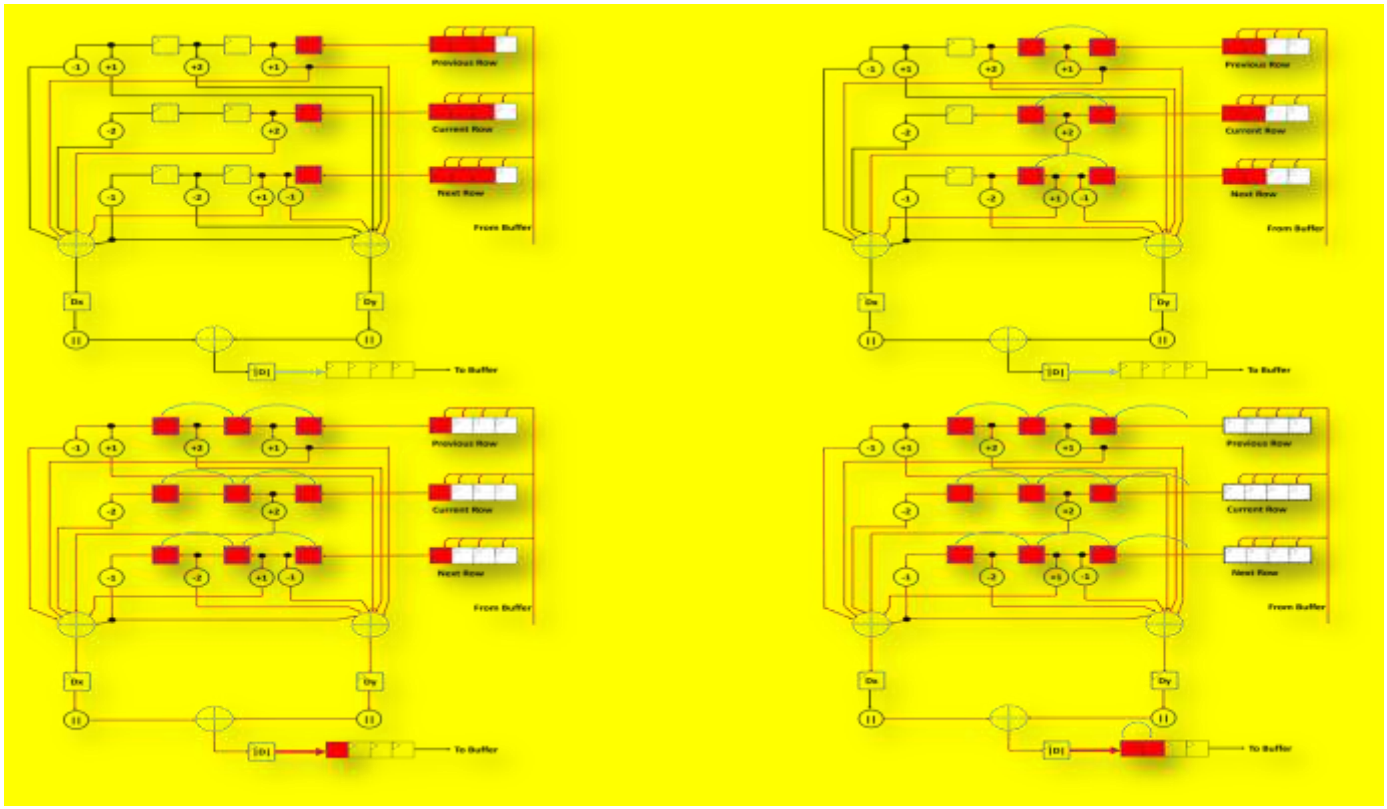

Fig. 7. Pipe-Line Data Flow

Hardware Platform Advanced Surveillance: Moving from simple motion detection to smart behavior analysis, such as quick facial recognition and detailed object tracking.

Hybrid Architectures: There's a growing use of System-on-Chip designs that mix ARM processors with FPGA logic, offering more flexible hardware-software co-design. Core Implementation Work flow to implement these algorithms, designers follow a structured, hardware-focused process.

Hardware Modeling: Using like Xilinx System Generator or MATLAB/Simulink to design systems without writing raw RTL code.

Tools HDL Development: Writing Verilog or VHDL to create logic gates, buffers, and memory structures such as Line Buffers and FIFOs. Testing the design in environments like ModelSim or Vivado Simulator to make sure timing and pixel accuracy are correct before using the hardware.

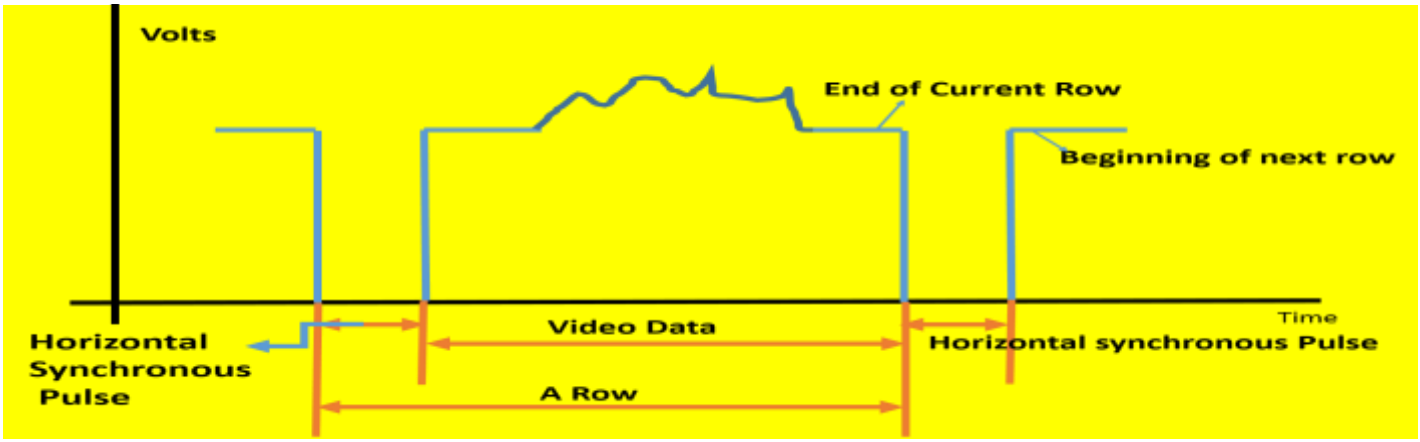

Fig. 8. Real Time Video Processing Systems

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Hardware Synthesis: Converting the code into a bit stream that sets up the physical FPGA logic blocks and DSP slices. The design developed will generate signals similar to that of a video acquisition system. In order to simulate a camera module, the characteristics of the camera output signal need to be studied. A composite video signal representing a single row of a frame from a camera is shown in figure. As the figure indicates, the composite signal contains both the video and synchronization signals. At the end of each row, a horizontal synchronous pulse will be generated, which will inform the following processor about an end of row event.

At the end of Each frame, a vertical synchronous pulse will be generated. In other words, a horizontal synchronous pulse will differentiate between different rows in a frame, whereas a vertical synchronous pulse will differentiate between different frames. There is another class of synchronization pulses that are used to retrace from one end of the row to the beginning of the next row. In normal FPGA based image processing systems, this event can be ignored. The generated signal will be fed to the input of an FPGA based parallel processor. In digital perspective, the signals will not be superimposed. The horizontal, vertical synchronous pulses and the data will be given as separate inputs to the processor, as in figure. New "parallel dual template" methods for filtering can improve performance by more than 600 times compared to software and double the speed of older single-template FPGA designs.

D. Embedded Image Processing

The threshold value used to detect edges should be calculated differently for each frame. The system should show the processed frames on a display, with the detected edges highlighted in white. In the simulation environment, a model should be created to imitate the behavior of a digital camera (Acquisition System).The image data should be converted into signals that are the same as those from a real camera. The image processing module, which is based on an FPGA, should be simulated using a software platform. This module should take inputs from the camera simulation model, generate the frame with detected edges, and display it in image or video format using a Graphical User Interface (GUI). The goal is to achieve 50 frames the system.

E.System Through put

From the perspective of an embedded imaging system, through put is the number of pixels processed in a single clock pulse. More than one pixel operation requires more time and a slower clock speed, which decreases the overall system speed but increases throughput. Higher system throughput can be achieved through multi-stage pipelined designs. In such designs, while the current pixel is in its final processing stage, the previous one might be in the second-to-last stage. So the number of pixels processed in one clock cycle depends on the number of pipeline stages. Each pipeline stage should have the same timing to achieve maximum throughput. System bandwidth is the total memory usage of the system in one clock cycle. High system bandwidth can reduce system efficiency. System bandwidth can be optimized using cache memories. Sequential image processing uses a computer system that follows a single path for processing. It breaks these instructions down into math and logic tasks that are handled by the ALU. A lot of speed can be gained if the processors don't have to wait for data from other stages. But the overall system can be faster because while one processor is working on data, another is already handling part of it. Data can be sent to the output device before all the steps are finished, which helps reduce the total time it takes.

Table .III LUT AND BRAM, DSP

Resource	Best Used For	Over-Utilization Result
LUT	General logic, small counters, multiplexers (MUXs)	Routing congestion and timing violations (failed timing)
BRAM	Large buffers and look-up tables for constants	Fallback to LUT-RAM, resulting in high area cost
DSP	Multipliers, multiply-accumulate units (MACs), and complex arithmetic	Logic-based multipliers, leading to slower performance and larger area usage

IF the algorithm’s steps depend on each other, this can cause delays and add extra work to transfer data between them.
So, it’s important to turn as many of these sequential steps into parallel ones. each one is mapped to a specific

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hardware setup or circuit. This mapping process is done for all the identified parallel parts. Next, these individual circuits are combined, and the communication needed between them is studied. Putting all these circuits together leads to the final result. After setting the overall structure for the parallel parts of the algorithm, the next step is designing the sequential parts. Here, we estimate how much data needs to be moved between the parallel parts. If the chosen board also has special features like carry logic, pipelined multipliers, and ALUs, the performance can be even better. High-end FPGAs with these advanced features are very expensive. In image processing design using FPGAs, high system bandwidth can cause delays and create bottlenecks when handling pixels.

FPGA Mapping Techniques

efficiently image processing operations are assigned to FPGA resources. These are standard ways to achieve the desired performance in terms of speed, memory, and resources. During the initial design phase, a list of constraints and methods to improve system efficiency is made. Three main constraints need to be handled when mapping sequential algorithms onto an FPGA time, bandwidth, and resource constraints. Time Constraints In real-time applications, the rate at which data arrives is a major issue. Low-level pipelining is one technique used to handle this problem Pipelining divides an operation into smaller stages and completes it in several steps clock cycle. Since only a part of the operation is done in each clock cycle, the overall clock speed can be increased. Therefore, more than one cycle is needed to complete one operation. If this hardware is duplicated, multiple pixels can be processed at once.

$$y = ax^2 + bx + c \text{……..(1)}$$

This equation can be implemented using one, two, or four-stage pipelines. the best latency is achieved with a two-stage pipeline, which improves the system throughput. the two-stage pipeline is most efficient because the addition and multiple operations are evenly distributed between two stages. In a four-stage pipeline, stages one and three involve multiplication operations, while stages two and four involve addition operations.

RESULTS AND DISCUSSION

Design Workflows and Speed: As FPGAs get more complex, design times become too long, so better CAD tools are needed. High-Level Synthesis (HLS): Making HLS tools as good as manual design, especially with good results for deep learning and demanding computing.

Security and Trust: Making systems more resistant to radiation and errors in space, using methods like Triple Module Redundancy. They are useful in IoT and edge AI applications by letting custom hardware handle data processing while controlling tasks are done with embedded processors.

Edge AI Inference: Optimizing neural network models for quick inference on edge devices. Using special logic for encryption, secure boot, and being ready for future quantum- based threats.

DSP Blocks and Memory: Special blocks that improve performance in digital signal processing and handling large data amounts. These are used to save the state of information in circuits that process data step by step. These are designed for fast math operations like filtering signals. These are circuits that connect the internal logic of the FPGA to the outside world. The FPGA-based implementation of the Sobel edge detection algorithm demonstrates significant performance improvements over traditional software execution. In software, an entire frame is usually processed at once. But FPGAs work best when processing a continuous flow of pixels. Storing complete frames in on-chip Block RAM (BRAM) uses a lot of resources, so designers use line buffers to store only the rows of pixels needed for operations like filtering. These benefits make FPGAs suitable for areas where delays are not acceptable, such as medical imaging, autonomous robots, and industrial surveillance. If the system often uses off-chip memory, it can slow down the system's response time and increase latency. Double Buffering is used in FPGA mapping to lower the number of memory operations. It is used between two image processing steps to avoid a bottleneck when using shared memory. This technique is commonly used with pipelining or with random access processing. Data is processed right away and stored in a buffer for random access processing.

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This technique works well between the streaming and random access processing paths. It uses two connected memory banks, as shown in Figure. The upstream process takes data from the input and writes it to one memory bank. The downstream process reads data in parallel from the other bank and displays it. When a frame is done, the roles of the two memory banks switch, so the data that was just uploaded by the upstream process is now ready for the downstream process. As a result, one frame period is added to the system's latency. One way caching is used in image processing operations is called row buffering. It stores the most commonly used data or results from earlier operations. On an FPGA using a cache can help reduce system delays. This helps lower the amount of data that needs to be transferred, reducing the system's bandwidth usage. In some setups, there are separate caches for data and results meaning one stores regular data and the other keeps the computed results. In certain applications, the cache is positioned next to the processor and the main memory, as shown in Figure. The needed system settings were calculated, and the way to build it was explained in earlier sections. The Use of image processing algorithms on FPGAs is a strong alternative to CPUs and GPUs, especially when dealing with high-resolution, real-time tasks that need low power and a lot of parallel processing. For example, a SIFT-based key point detection on 2048x1088 high-resolution images can complete in just 33 milliseconds, which is almost 10 times faster than software-based versions.On-chip memory (Block RAM) is a major limitation. it might not be enough to hold the entire image, so off-chip memory like SDRAM or DDR is often needed, or efficient line buffering is used for processing small parts of the image.

Verify via Hardware-in-the-loop (HIL): Combine initial simulations with HIL testing to make sure the algorithm works well with real-world sensor noise and timing issues that software simulations might miss. Implementation Resource Comparison A full image processing pipeline, such as Bayer - DoG -SIFT - Matching, can use a large portion of an FPGA's resources. Producing digital images with good brightness, contrast, and detail is a strong requirement in several areas like vision, remote sensing, biomedical image analysis, and fault detection. Creating visually natural images or transforming images to enhance the visual information within them is a primary requirement for almost all vision and image processing tasks. Medical imaging applications where contrast enhancement and sharpening are needed can also benefit from this work. Potential areas of application include digital X-ray, digital mammography, CT scans, and MRI. The same image enhancement techniques can be applied to RGB color images instead of gray scale images for manual and automatic color correction. These techniques are also called point processing techniques because they are applied directly to individual pixels. In this project, these image enhancement techniques have been taken for VLSI implementation on FPGA hardware. Work, a methodology for designing algorithms for efficient implementation has been presented and evaluated.

SUMMARY AND RECOMMENDATIONS

Any future FPGA-based real-time designs can be integrated into realsim. An immediate enhancement to this simulator would be the addition of video processing features. Furthermore, other edge detection algorithms like the Laplacian of Gaussian, Canny edge detectors, and others can be added to the edge detection feature of the simulator. An option to compare the performance of similar image processing techniques would help the designer choose the best implementation strategy and would make the simulator more professional. In addition, the current design can be extended to implement more complex algorithms like the Viola-Jones face detection algorithm and optical flow. These implementations involve a significant amount of sequential operations in the algorithms. Special strategies should be employed to reduce the effects of communication overhead.

The work presented here has a wide scope and various applications. Edge detection techniques are basic steps in several complex computer vision applications. The implementation of fast face detection in a digital camera, fast object tracking, policing, and interactive surveillance, and finally applications like object tracking and chasing are some of the areas where this work can be used. more importantly, this work will serve as a motivation to explore the endless possibilities of FPGA-based computer vision designs. To use less power than general-purpose processors by employing methods like gated clocking for parts of the system that are not in use.

Image Pre-processing: Converting images to gray scale, enhancing contrast, adjusting brightness, reducing noise (using Median or Mean filters), and changing color spaces (like from Bayer to RGB).

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Compression & Transforms: Using Discrete Cosine Transform for video compression. Through put & Latency: Measuring how many pixels are processed per clock cycle and the total time taken for image processing.

Conformed to, making it the lowest common denominator that all PC graphics hardware supports before a device-specific driver is loaded into the computer. This VGA controller creates three color signals red, green, and blue and two control signals Hsync and Vsync. The analog levels on the color signals, which range from 0 volts (completely dark) to 0.7 volts (maximum brightness), tell the monitor what intensities of these primary colors to use. Each analog color input can be set to one of four levels using two digital outputs. So a pixel can have one of 64 different colors and only 4 shades of grey. Results Simulation result the simulation result for negative transformation. Here, the input pixel values are inverted, meaning they are subtracted from 255.Here, input pixel values are changed to either zero or 255 based on how they compare to the threshold, as explained before. The threshold used here is set to 64. the simulation result for contrast stretching. Here, input pixel values are stretched towards either zero or 255 by comparing them with two thresholds. If the pixel values fall between these two thresholds, they are kept as they are. The thresholds used in this case are 64 and 150.

Traditional HDL simulators like Modalism, Xilinx ISE, etc., display simulation results in the form of binary waves. If the circuit is not very complex, it is not too hard to understand the binary waves. But most image processing operations are complicated and involve a lot of signals. So it becomes really hard to understand the results of image processing from binary waves. This was the main reason for creating a new simulation platform. The simulation of any FPGA-based image processing algorithm has three main parts. A test bench to simulate an image acquisition system. An image processor A test bench to simulate a display device. Putting all three parts together effectively is important for making the design clear and easy to repeat. The new simulator called realism combines all three parts and offers better visual results compared to traditional HDL simulators.

All the background work is done in HDL. The simulator shows the background work in a status bar. Realism provides three different ways to view input and system output. As an image in the image window As a hex-image file As binary waves .These three views help in understanding the design and the underlying ideas. Also, they make it easier to trace back and debug the design. Integrated Waveform Analysis Realism shows the simulation results as images output in more detail, like simulation events and their timing, you can use the waveform view. In this window, the output is shown as binary. Realism offers better visual perception and additional features compared to traditional HDL simulators. Realism can be used for any FPGA-based real-time image processing applications, like face detection or object tracking. Also, the simulator can be improved by adding the ability to use real-time video input. In the future, this simulator could become a standard tool for validating FPGA-based real-time designs image in the image window As a hex-image file As binary waves .These three views help in understanding the design and the underlying ideas. Also, they make it easier to trace back and debug the design. Integrated Waveform Analysis Realism shows the simulation results as images output in more detail, like simulation events and their timing, you can use the waveform view. In this window, the output is shown as binary. Realism offers better visual perception and additional features compared to traditional HDL simulators. Realism can be used for any FPGA-based real-time image processing applications, like face detection or object tracking. Also, the simulator can be improved by adding the ability to use real-time video input. In the future, this simulator could become a standard tool for validating FPGA-based real-time designs

The test points compare the results of the original algorithm run in MATLAB with the results from the modified algorithm implemented in FPGA. In the current situation, most real-time application are implemented either in micro-controllers or DSP processors. For example, most digital cameras on the market use micro-controller based pre-processing circuits. Moreover, in the world of portable devices and gadgets, it is very important to use less power for longer battery life. From an image processing perspective, the speed of execution is a direct measure of power consumption. To achieve the least power consumption, the sequences should run in the Fewest number of clock cycles. The final goal of any FPGA-based design is to convert it into an ASIC (Application-Specific Integrated Circuit). The process of changing an FPGA-based design into an ASIC is time-consuming and expensive. These extra efforts and costs are the reasons why FPGA-based designs are not

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widely used in the current industry, especially in countries like India. This work can serve as a motivation and a gateway to the exciting area of research in FPGA-based computer vision.

Power analysis

Total, including dynamic, static, and bias power. This can be done through simulation after design is done (like after synthesis or place-and-route)or by using physical measurement tools like Xilinx Power Estimator (XPE) and Intel's Power and Thermal Calculator help estimate power based on how active the design is. Good analysis helps find circuits that change a lot (high toggle rate) to stop overheating and protect against attacks that use power data. Dynamic Power Depends on capacitance, voltage, and frequency. Static Power Comes from leakage current and is affected by temperature, usually following a complex exponential pattern. Bias Power Related to circuits used to set the right voltage levels. Pre-Implementation Estimation: Early guesses using tools like XPE or spread sheets based on how much resources the design uses.

Post-Implementation Estimation: Tools like Quartus Prime Power Play Analyser use real net lists and simulation results to find exact toggle rates. Physical Measurement: Using probes or built-in circuits to measure how much current is being used through a resistor in the power supply. Often take up 50–70% of the total dynamic power in designs like Xilinx Virtex-II. Power analysis is also used to check if encryption is secure, because dynamic power changes linearly with the number of switches in flip-flops. While GPUs offer massive throughput for specialized workloads, CPUs remain essential for overall system control and tasks with complex dependency chains. Innovations in architecture Right now, people are working on improving FPGA designs to make them more efficient, so they can compete with ASICs. But they still want the flexibility of reconfigurable hardware. Some important changes include adding special "hard" parts for AI and fast communication. Also, there's a move toward using mixed systems that have both programmable parts and regular processors.

Register Retiming and Hyper Flex: These new techniques allow for more flexible placement of registers, helping to improve clock speed and timing, something that was common in ASIC designs before. For more detailed information on modern FPGA development, you can check out the Intel one API FPGA Handbook or AMD's Versal Adaptive SoC documentation. Resource Optimization and Management usually, aiming for around 70% is good, as it leaves room for changes or tools that help check the design. Estimation: Designers can use tools like Xilinx Vivado or LabVIEW FPGA to guess how much of the FPGA will be used without having to run a long process.

FPGA Timing Analysis:

Static Timing Analysis (STA): This analyzes all possible paths in the design without looking at actual input signals. It checks the worst-case situations.

They are usually written in SDC files and are important for accurate analysis.

Critical Path: This is the slowest path in the design that determines how fast the whole system can run. This is the difference between how much time a signal is allowed and how long it actually takes.

Paths Analyzed: These include connections between registers, inputs and outputs that connect to other devices, and control paths that handle unusual signals.

Setup/Hold Check: This checks when data is sent and received to make sure it's not too early or too late, which can cause problems with data handling.

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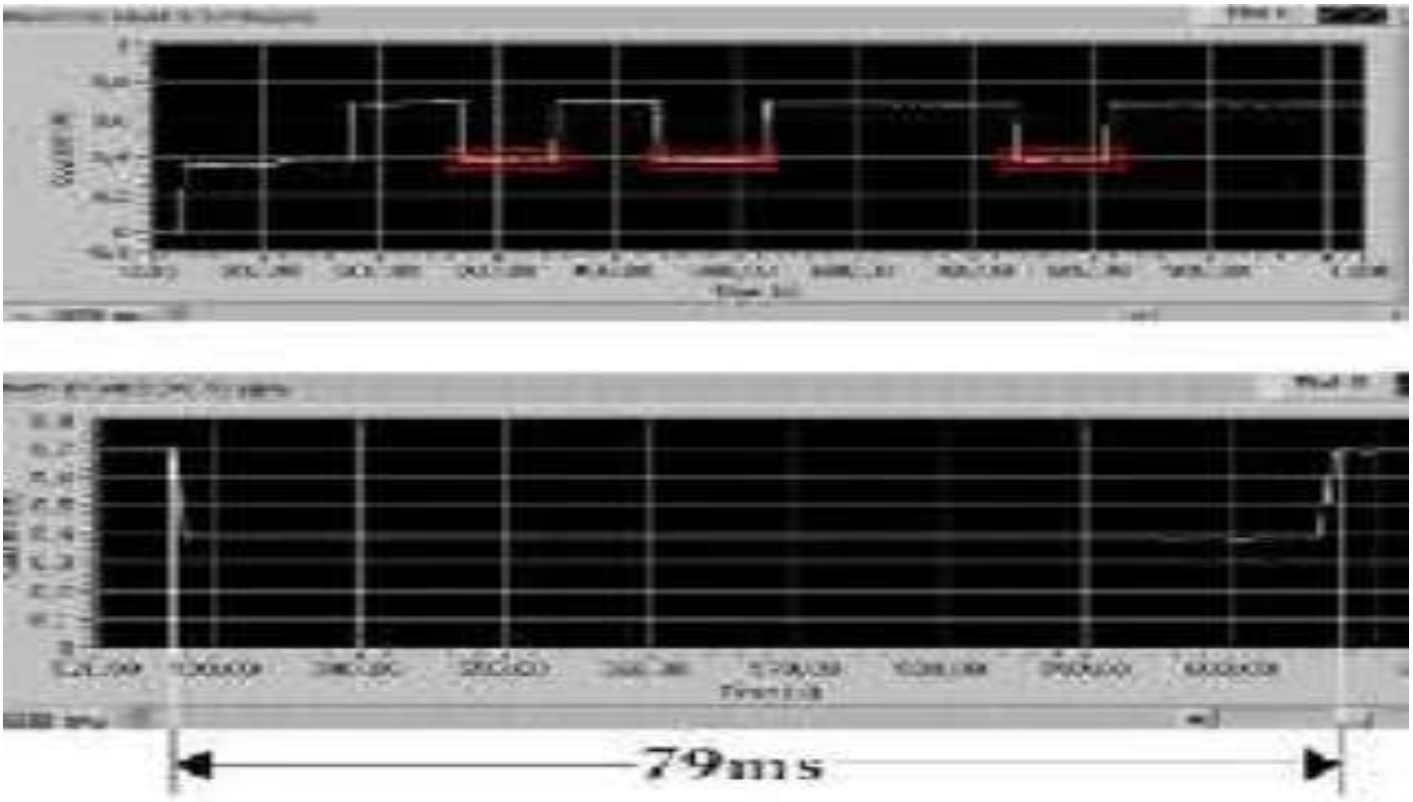

Fig.9. Wave Form Output

Reduce Logic Levels: Simplify the logic between parts of the circuit to make the signal paths shorter. Make longer paths shorter by adding registers at key points.

Improve Constraints: Make sure the clock settings, false paths, and how many cycles some paths take are correctly set.

CONCLUSIONS

FPGA-based implementation of image processing algorithms with a focus on real-time performance. By leveraging parallelism and pipelined architecture, the proposed system significantly outperforms traditional software-based approaches. FPGAs are better for systems that need special features, save power, or require fast responses (like edge AI). GPUs are better for general tasks that need lots of calculations, quick setup, and big computing power. They are used in areas like medical imaging, factory vision systems, satellite pictures, and self-driving cars. They are good at doing tasks that need very little delay, such as filtering, finding edges, and changing color formats. These tasks often use special hardware built using HDL or High-Level Synthesis (HLS). Used for high-speed tasks like 2D convolution, edge detection, and changing brightness. Using specific filters to speed up inspections and cut down on cycle times, which is often faster than GPUs. Medical Imaging: Speeding up image **analysis to help in real-time diagnosis.**

Recommendations: Future work should focus on migrating these algorithms to SoC-based platforms to leverage the flexibility of software with the speed of hardware. Additionally, exploring hardware-accelerated machine learning models could further enhance the capabilities of this system." The implementation of Sobel edge detection demonstrated substantial speed improvements, confirming the effectiveness of FPGA-based designs for high-speed image processing applications. The architecture is scalable and can be extended to more complex algorithms such as object detection and machine learning-based vision systems. FPGAs can run many operations or process different image sections. Superior Speed and Efficiency: The future of this field is moving towards integrating AI, where FPGAs act as efficient accelerators for deep learning and AI Acceleration, neural networks.

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Edge Computing in Healthcare: medical devices that provide real-time help during surgery and automated diagnosis in telemedicine. FPGAs allow for changing or updating algorithms quickly without changing the physical hardware, helping reduce time-to-market and prevent obsolescence. Both VHDL/Verilog(RTL) and High-Level Synthesis (HLS) are standard ways to implement Sobel Edge Detection on FPGAs, each offering different trade-offs between design control and development speed.

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"This research concludes that the modern implementation of image processing algorithms on FPGA provides a robust and efficient solution for real-time data processing. By leveraging High-Level Synthesis (HLS), the design process was significantly accelerated while maintaining high resource efficiency. The experimental results demonstrate that the FPGA-based system provides deterministic latency and lower power consumption compared to traditional software-based approaches. This makes the proposed architecture highly suitable for high-speed embedded vision applications such as autonomous navigation and industrial automation."

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