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Design of Low-Power ÷16/17 Prescaler Using Powerpc Flip-Flops

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Abstract: Pre-scalar, this is considered as the most critical block in the design of frequency conflation plays veritably important part, whenever we talk about high frequency operation. These blocks are used generally in PLLs for frequency conflation. Rigorous trials have proved that the major donation for power dispersion in ADPLL is because of pre-scalar block. Hence it becomes veritably pivotal to design the pre-scalar block with minimal power dispersion. In this paper we borrow a fashion of using Power PC flip-flop to design a divide by 16/17pre-scalar, which consumes veritably minimal power. The propound circuit operates up to 1 GHz consuming veritably lower power of 0749mW. The affair frequency is in the range of 50 MHz to 60 MHz. Low power peak by 16/17pre-scalar using Power PC flip bomb is proposed at 0.12 µm CMOS technology using BSIM4 model at a force of 1.2 V. The circuit is schematically vindicated in DSCH 3.8. The layout verification was carried out in Microwind2. From the simulation it was observed that veritably minimal power dispersion was attained with a minimal face area of 1875.9 μm^2.

Keyword: Power PC flip flop; Pre-scalar; dual modulus; frequency synthesis; ADPLL

I. Introduction

With an ever increasing scaling factor and technology, the system conditions have reached a stage which demands advanced processing and high speed of operation. The revolutionized use of mobiles and its affiliated products has given rise to the challenge of achieving advanced battery life. One similar element which directly relates battery life or power consumption in mobiles is the Digital Phase locked loop or frequency synthesizer to be on broader note. Theprime element which adds on to the device power consumption is the Pre-scalar, therefore the genuine design of pre- scalars which operate at high speed, consuming minimal power is getting veritably consequential in recent times. For any pre-scalar system, the flip- duds come the core element and the proper usage off lip- bomb results in a power effective pre-scalar. For numerous of the flip- duds which are continues in nature, design methodologies which help in power reduction play an important part. All this has to be without altering the originality of the flip- bomb armature.

High- speed and low- power operation has been successfully achieved in coetaneous bias through the use of pipelining styles. still, deep pipelined systems similar as those employing multiple flip- duds and latches present significant design challenges. thus, when designing a circuit that performs efficiently in terms of both power and speed, the proper selection of the flip- bomb armature plays a pivotal part. Several experimenters have proposed colorful prescaler infrastructures, yet utmost of these designs continue to calculate on conventional flip- bomb structures. The necessity to develop prescalers grounded on indispensable flip-bomb infrastructures with minimum power consumption serves as the primary provocation for this work. While high- speed operation has been demonstrated in numerous prescaler designs using different types of flip- duds, the predominant sense style employed for achieving high operating frequentness is MOS Current Mode Logic(CML). Although effective in speed, CML circuits fall under the order of high- power consumption designs. On the other hand, True Single- Phase timepiece(TSPC) sense-grounded prescalers(1),(2) parade reduced switching power but operate at fairly lower frequentness. The Extended True Single-Phase timepiece(E-TSPC) sense style(3) farther improves the operating frequence but suffers from increased short- circuit power dispersion, making it less suitable for low- power operations. In moment's period of high- performance systems, minimizing power dispersion — both dynamic and stationary — has come an essential design demand. Prescalers, being critical factors in Phase- Locked circles(PLLs) and frequence synthesizers, frequently operate at maximum frequentness and therefore contribute significantly to total power consumption. To address this issue, the proposed work introduces a new binary- modulus peak- by-16/17 prescaler grounded on the PowerPC flip- bomb topology. This design aims to achieve minimum power dispersion while maintaining high- speed performance.

Overview Of Flip-Flop Topologies

Extensive research has been conducted on various types of flip-flops and latches in recent years. Broadly, these designs can be classified into **static** and **dynamic** styles. The static design category includes master–slave architectures such as the **C^2MOS flip-flop**, **transmission-gate (TG) based master–slave flip-flop** [4], and the **PowerPC 603 logic-style master–slave flip-flop** [5].

An innovative master–slave circuit, presented in [6], is the **C^2MOS flip-flop**, which operates in two distinct stages. This positive edge-triggered flip-flop functions during both clock phases (CLOCK = 0 and CLOCK = 1), where the master and slave alternately switch between evaluation and hold modes. Its application in constructing a divide-by-15/16 prescaler was demonstrated in [7].

Given the availability of multiple flip-flop variations, selecting an appropriate design depends on the **performance requirements** of a specific application. It is, therefore, incorrect to label any particular flip-flop as inefficient without considering its **intended**

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functional context. For the design of a **low-power, multi-modulus prescaler**, it becomes essential to choose a flip-flop architecture that ensures **minimal power dissipation**.

Figure 1 illustrates the power dissipation characteristics of various flip-flops operating at 10 MHz [8].

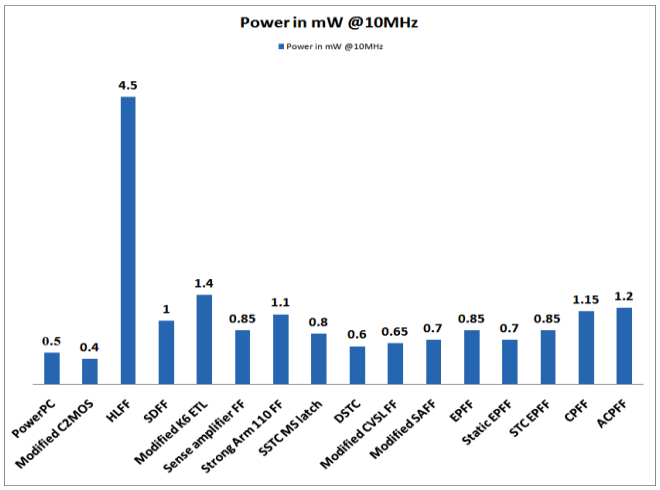

Fig. 1. Power dissipation of various flip-flops [8]

In the case of **dual-edge-triggered (DET)** flip-flops, both power dissipation and critical path delay are generally higher than those of **master–slave C²MOS** designs. The **hybrid latch flip-flop (HLFF)** and **semi-dynamic flip-flop (SDFF)** architectures perform better in terms of clock skew and timing latency [1], [9]. However, the **large hold time** associated with HLFF designs may lead to **race conditions**, adversely affecting power performance. The **sense amplifier flip-flop (SAFF)**, with a smaller hold time, alleviates this issue, but its **asymmetric delay paths** cause longer clock-to-output delays [8].

A major contributor to power loss in **semi-dynamic circuits** is the **large pre-charge capacitance** and **redundant data transitions**. An attempt to minimize this redundancy was presented in [10], where the pre-charge nodes were controlled by pull-up and pull-down transistors. However, this configuration still resulted in high pre-charge capacitance.

In **dynamic logic flip-flops**, performance improvement is often achieved due to the presence of a pre-charge node [9], [10]. Nevertheless, this same node introduces **substantial node capacitance**, which limits their suitability for **low-power applications**. Among dynamic structures, **pulsed designs** and **TG-based flip-flops** are recognized for their efficiency in **high-speed applications** [8].

From Fig. 1, it is evident that the **modified C²MOS** structure offers high efficiency in terms of power performance. However, when compared to the **PowerPC 603** flip-flop, the latter provides advantages such as **direct data paths**, **minimal latency**, and **reduced power dissipation**, making it a strong candidate for prescaler design.

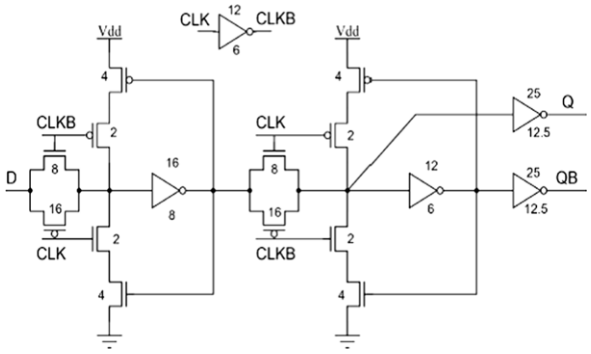

Fig. 2. Schematic of PowerPC 603 flip-flop

A detailed analysis of various flip-flop architectures [6] indicates that the **PowerPC 603 flip-flop**, as shown in Fig. 2, outperforms others in terms of **power–delay product (PDP)**. Furthermore, for circuits with **data activity below 40%**, the PowerPC 603 architecture demonstrates superior efficiency [11].

Although the **C²MOS** flip-flop exhibits relatively low power dissipation, the **PowerPC 603** flip-flop is preferred in this work due to the **transmission-gate-based structure** commonly used in prescalers. This TG configuration in C²MOS introduces **additional dynamic power losses**, which makes PowerPC 603 a more **optimal choice** for achieving low-power operation in frequency synthesizer applications.

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Table1. Power dissipation comparison between PowerPC 603 flip-flop and C²MOS flip-flop.

Output Voltage	Powerdissipation(mWatt)	
	PowerPC603FF	C²MOSFF
0.200	**1.249**	0.428
0.400	1.235	0.433
0.600	1.221	0.769
0.800	1.169	**0.803**
1.000	0.679	0.501
1.200	0.003	0.070

Traditional And Suggested Dual-Modulus Prescaler

The traditional divide-by-16/17 prescaler is illustrated in **Fig. 3**. Theoretically, it is difficult to precisely estimate the working period based on the critical path delay, as results vary across different design tracks. Consequently, there exists a trade-off between the lengths of the two most critical paths. In this work, the main objective is to **minimize power dissipation** by **reducing the length of the critical path**.

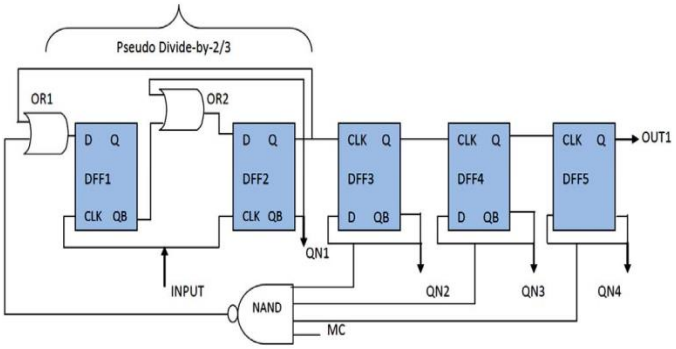

Fig. 3. Traditional divide-by-16/17 prescaler.

The **suggested divide-by-16/17 prescaler** is shown in **Fig. 4**. On the first positive edge of the input signal (INPUT), the nodes QN0, QN1, QN2, and QN3 rise for one, two, four, and eight clock pulses, respectively. On the second positive edge of INPUT, the signal **MC1** goes high and remains high for one clock period. When the second positive edge of INPUT arrives, QN1 transitions low for one period. During the third positive edge, QN0 and AND2 go low and hold their state for one period. A divide-by-three signal is observed on QN1 from the third to the ninth positive edge of INPUT, thereby achieving a **divide-by-3 operation**. Ultimately, a **divide-by-17 output** appears at node **OUT1**.

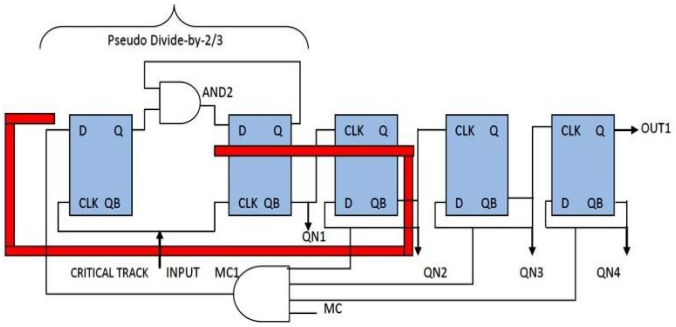

Fig. 4. Suggested divide-by-16/17 prescaler.

The entire schematic is implemented using the **PowerPC 603 flip-flop**. The **timing diagram**, shown in **Fig. 7**, clearly demonstrates the behavior of INPUT, QN2, and AND2 signals, which go low irrespective of QN0. The MC1 signal remains high before the third positive edge of INPUT. This is achieved by driving QN1 low such that the AND2 signal retains its previous state. The signal path that includes MC1 forms the **critical track** of the proposed design, as depicted in Fig. 4.

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It is essential that the signal propagating through the critical track completes within one period of INPUT. The critical track of the suggested circuit includes **FF1**, **FF2**, and **AND1**. The **minimum period (T_{min})** of the proposed prescaler can be expressed as:

Tmin_Suggested=(td_QN,DFF1+td_QN,DFF2+t"setup,DFF0)/2

To summarize, the operation of this **multi-modulus prescaler** can be defined as follows:

- When **MC = 0**, the prescaler functions as a **divide-by-16** circuit.
- When **MC = 1**, it operates as a **divide-by-17** circuit.

The **working frequency** of the proposed prescaler is primarily determined by the operation of the divide-by-17 mode.

Fig. 5 illustrates the multi-modulus prescaler previously proposed by **Huimin Liu, Xiaoxing Zhang, Yujie Dai, and Yingjie Lv [7]**. The main drawback of their design was **high power dissipation**, largely attributed to the **multiplexer (MUX)** located in the critical path. In the proposed design, this issue is mitigated by replacing the MUX with **two AND2 gates**, thereby reducing power consumption and critical path delay.

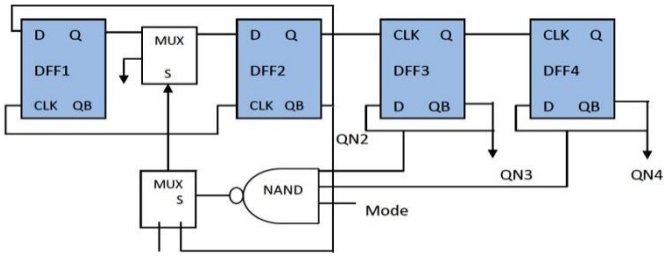

Fig. 5. Divide-by-16/17 prescaler proposed by [7].

The **layout of the PowerPC 603 flip-flop**, used in constructing the suggested prescaler, is shown in **Fig. 6**. The total **layout area** is approximately **1875.9 µm²**.

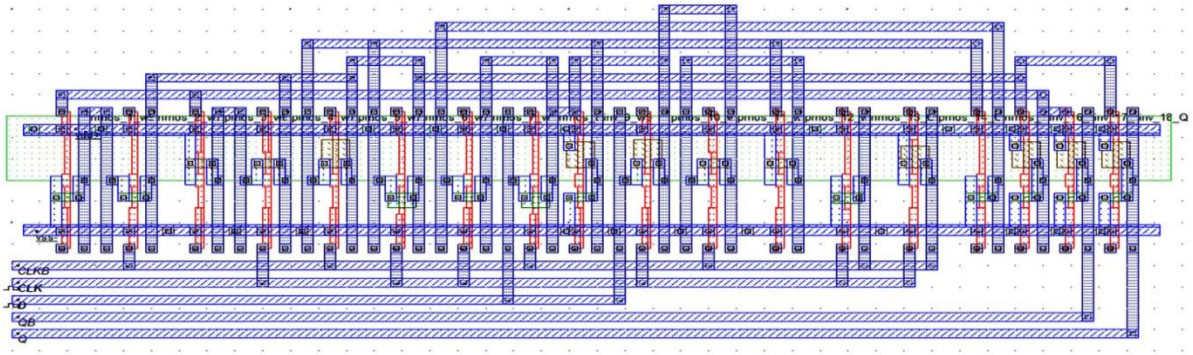

Fig. 6. Layout of PowerPC 603 flip-flop used in the suggested prescaler.

The **timing diagram** for the divide-by-16/17 prescaler is shown in **Fig. 7**, which verifies the expected logical transitions of the design.

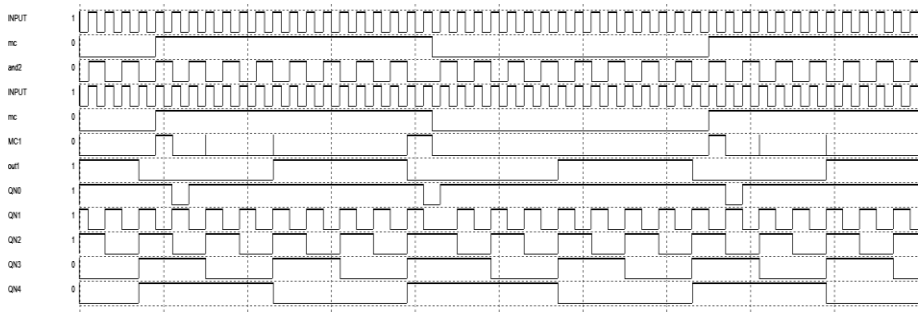

Fig. 7. Timing diagram of divide-by-16/17 prescaler.

The **post-layout simulation waveforms** are shown in **Fig. 8**, which closely match the schematic results. **Fig. 9** and **Fig. 10** present the current–voltage (I–V) characteristics at the **input** and **output** sides, respectively, for the proposed prescaler. The **power dissipation analysis** at an input frequency of **1 GHz** is illustrated in **Fig. 11**.

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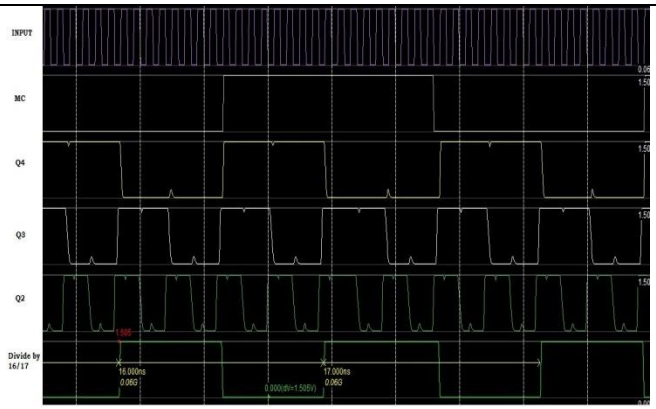

Fig. 8. Output waveform of the layout of the suggested prescaler.

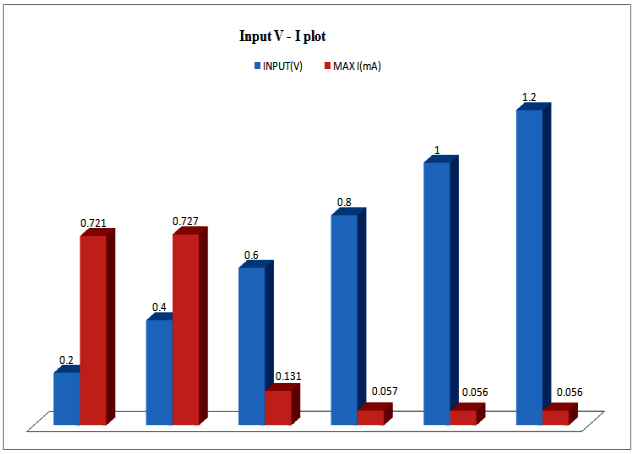

Fig. 9. Input V–I graph of the suggested prescaler.

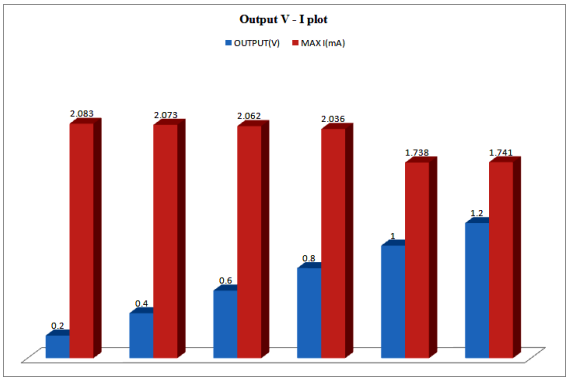

Fig. 10. Output V–I graph of the suggested prescaler.

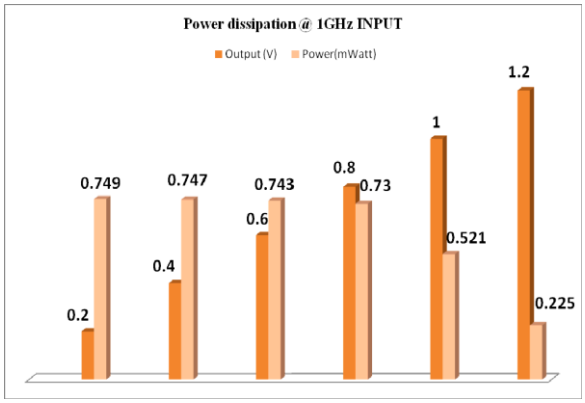

Fig. 11. Power analysis of the suggested divide-by-16/17 prescaler.

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The plot in Fig. 9 clearly demonstrates the **saturation of current in the transistors** for input voltages above **0.6 V**.

The overall observations confirm **significant improvement in power efficiency** owing to the use of the **PowerPC 603 flip-flop**. The results indicate reduced power dissipation and area consumption when compared to conventional prescaler architectures. **Table II** summarizes the performance comparison of the proposed circuit with previously reported designs.

Table II – Comparison of the Proposed Circuit with Previous Works

Publication	TSCAS-I	TSCAS-II	TICCM[7]	This Work
Year	2010	2011	2011	-
Type	TSPC	TSPC	TSPC+TG	PowerPC
DivideRatio	32/33	7/8/9	15/16	16/17
Frequency	1.5~4.5 GHz	3.4~5 GHz	0.5~3.125 GHz	~1GHz
Power(mW)	2.2	1.6	4.23	0.749
Supply	1.8	1.2	1.8	1.2
Process(μm)	0.18	0.18	0.18	0.12

II. Results

The simulation of the suggested pre- scalar was carried out on DSCH 3.8 tool for schematic analysis, the layout of which was vindicated on microwind2 tool. With a maximum operating frequency of 1GHzandmaximumoutputfrequencyof 60 MHz under 12V power force; standard 0.12 µm CMOS technology was used. A working period of 16.66 ps and a power dispersion of 0.749 mW is achieved which is veritably effective when compared with other pre-scalars. The results are presented as shown in separate tables and numbers. The overallsurfaceareaof1875.9µm2forpre- scalar and an overall face area of 234.7 µm2 for PowerPC flip bomb were achieved.

III. Conclusion And Futurescope

The work presented in this paper bandied about a Low power divide- by- 16/ 17prescalarusingPowerPCflipflop. The main end of this work was to apply a new multi- modulus separator circuit with veritably minimal power consumption. The work carried out presented a brief about why we go for power PC flip bomb rather of other flip bomb performances. Proper selection of W/ L rates of power PC flip bomb gave us a mimium power dispersion in such a manner that it, was made stylish suited for multi modulus pre-scalars. Simulated in 0.12- µm CMOS technology, the power Pc pre-scalar circuit achieves a affair frequency in a range from 50 MHz to 60 MHz. The maximum operating frequence is 1 GHz The power consumption is 0.749 mW at 1.2 V force voltage. The projected circuit can be analysed for its advancements using same conception for advanced peak values. With veritably low power dispersion and minimal current, it can be said that this particular circuit is suitable for low power operations. The projected circuit can be extended a) To make advanced interpretation binary modulus pre-scalar with exactly same topology but by adding the number of flip- duds. b) by using other low power flip- bomb topology to gain lower power dispersion. c) To gain pre-scalars with two different flip- duds ina single armature, performing into mongrel pre-scalars.

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Biography

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