

Optimized 2/3 Prescaler Design Using Different Logic Families in 45nm CMOS Process

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Abstract: Frequency division is a key application of flip-flops, particularly in wideband frequency synthesizers based on phase-locked loops (PLLs). In such systems, the high-frequency output from the voltage-controlled oscillator (VCO) is typically fed directly into a prescaler, also known as an $N/N+1$ counter, which serves as a critical building block. As semiconductor technology continues to scale down, both the channel length and supply voltage are significantly reduced. Consequently, the prescaler must operate reliably at higher frequencies and under lower voltage conditions.

Keyword: LT-Spice-IV, VCO (voltage-controlled oscillator), DMP (Dual Modulus Prescaler) TG (transmission gate), PTL (pass transistor logic).

I. Introduction

CMOS technology has remained the dominant integrated circuit platform for over 15 years, owing to its many benefits such as high integration density, low power consumption, high-speed performance, ease of design and implementation, cost-effectiveness, and straightforward simulation using software tools. With the ongoing scaling of transistor dimensions—specifically reductions in channel width and length—some of these advantages have been further enhanced. For instance, higher integration levels and improved operational speed have made CMOS suitable for applications that once required faster and more costly technologies like Bipolar or GaAs.

One significant area benefiting from these advancements is radio frequency (RF) circuit design, which includes systems for wireless communication and data transmission. Applications in this domain range from basic remote control systems, such as automatic gate openers, to complex devices like modern cellular phones. In advanced RF or wireless systems (such as Zigbee), one of the key components is the frequency synthesizer. This block generates precise frequency signals used for modulating and demodulating data within the transmission band.

A typical frequency synthesizer consists of a voltage-controlled oscillator (VCO), frequency dividers or counters, phase detectors, and filters. Some synthesizer architectures incorporate a dual-modulus prescaler ($N/N+1$), a type of frequency divider capable of dividing the input signal by either N or $N+1$, which is essential for achieving flexible frequency generation.

In general, the prescaler is a critical block in terms of speed and power consumption, as it directly receives the clock signal from the VCO output—the fastest signal in the frequency synthesizer. In this work, we present the design and simulation results of a 2/3 dual-modulus prescaler. The design utilizes the True Single Phase Clock (TSPC) technique or an alternative D flip-flop logic style, such as transmission gate logic, pass transistor logic, or Gate Diffusion Input (GDI) logic.

Additionally, novel circuit structures were implemented to enhance the overall speed of the design. The prescaler circuits were developed using LTSpice IV software based on 45nm CMOS technology. This paper presents three different 2/3 dual-modulus prescaler designs: the first utilizes the Enhanced True Single Phase Clock (ETSPC) technique and includes a detailed analysis; the second employs transmission gate logic; and the third is based on pass transistor logic. In the third design, the AND and OR gates are implemented using Gate Diffusion Input logic to further optimize further.

Prescaler architecture

The block diagram of the 2/3 prescaler architecture is shown in Figure 1. This dual-modulus prescaler combines both synchronous and asynchronous division techniques to reduce the input frequency, thereby simplifying the design and operation of the asynchronous, resettable modulo- P and modulo- S counters.

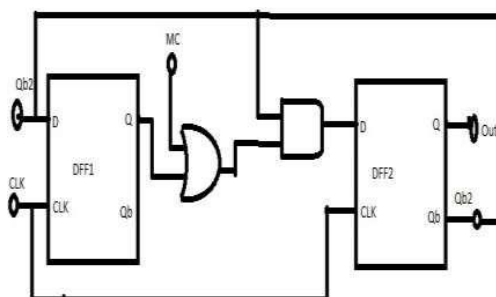


Fig.1: Prescaler Architecture

From a circuit topology perspective, prescalers and programmable counters are typically implemented using different logic families or various D flip-flop design styles, depending on their specific speed and performance requirements. Due to the differences in voltage levels between these blocks, a level shifter is often required after the dual-modulus prescaler (DMP) to ensure proper signal interfacing. The basic architecture of the programmable frequency divider is shown above.

Implimentaion or Design of D-Flip Flop Using Various Logic

In this chapter, we discuss the design of D flip-flops using various logic styles, including True Single Phase Clock (TSPC), pass transistor logic, and transmission gate logic. Each of these design approaches influences the overall circuit performance by reducing power dissipation, minimizing propagation delay, and enhancing reliability.

D-flip flop Using TSPC (True Single-Phase Clock)

Dynamic or clocked logic gates are employed to reduce circuit complexity, enhance operating speed, and lower power consumption. Among the various dynamic CMOS techniques, the True Single Phase Clock (TSPC) approach is notable for using a single clock signal, which minimizes clock skew—apart from inherent clock delay—and enables operation at higher frequencies. TSPC-based designs simplify clock distribution and eliminate issues related to phase overlapping. An additional advantage of TSPC is that it does not require multiple clock sources; it operates efficiently with a single clock, leading to reduced power dissipation.

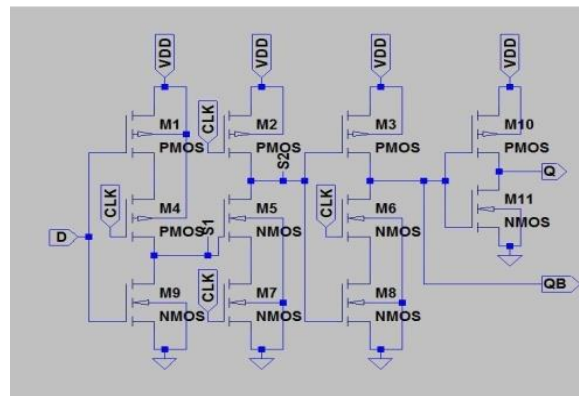


Fig.2: D-flip-flop using TSPC Logic

Figure 2 [9] illustrates a conventional dynamic TSPC D-flip-flop composed of nine transistors. To achieve higher speed, the clock-controlled switching transistors are positioned closer to the power supply or ground. The flip-flop changes its state on the rising edge of the clock signal, clk.

B.D-flip flop using Transmission gate

The D flip-flop circuit, shown in Figure 3, is implemented using transmission gates and inverters. The transmission gate is one of the most widely used CMOS structures in integrated circuit design due to its effective switching behavior, compact layout, and ability to simplify logic. In Figure 3, transmission gates T1 and T4 are turned ON, enabling signal transmission.

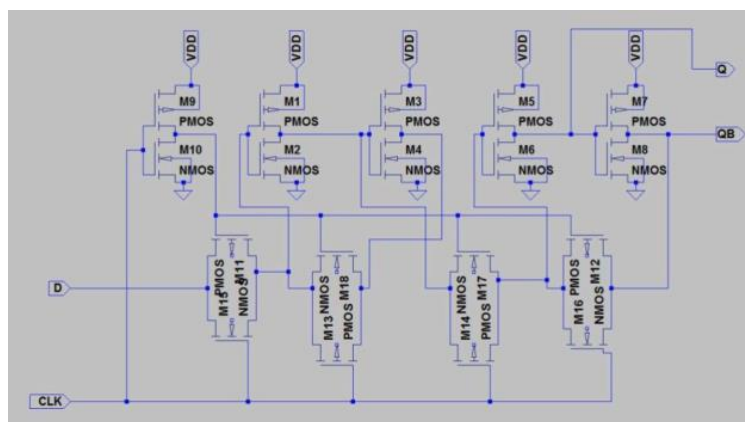


Fig. 3: DFF using Transmission gate Logic(TG)

At the falling edge of the clock, gates T2 and T3 are turned OFF. During this phase, the slave latch forms a feedback loop through inverters P3, P4, and T4, preserving the previously captured value from *Din*. Although the master latch captures the next input state at this point, it does not propagate to the slave since T3 remains OFF. When the clock transitions to the rising edge, T2 and T3 turn ON, allowing the newly latched value to pass to the slave via the loop formed by inverters P1, P2, and T2.

C. D-flip-flop using Pass Transistor Logic (PTL)

Pass transistor-based CMOS logic is well-suited for applications where high speed and high packing density are critical requirements.

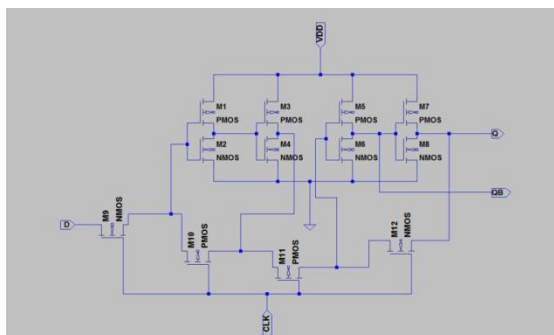


Fig. 4: DFF using Pass Transistor Logic (PTL)

The logic results in reduction in the number of transistors of the circuit by introducing differential logic and eliminating additional transistors. In pass transistor logic style we use either NMOS or PMOS transistor to build a design. Logic levels are passed between nodes of circuit as transistors are utilized as switches. The amount of active devices is thus reduced; however as the number of stages increase it becomes difficult to observe a significant difference between high and low logic levels. Master-slave latches have been implemented using inverters and pass transistor logic (PTL) as shown in figure4. The two chained inverters are in memory state when the PMOS loop transistor is on, that is when clock (clk) = 0. Other two chain inverters on the right hand side acts in the opposite way. The flip-flop changes its state during the falling edge of the clock.

Simulations Results of the 2/3 Prescaler

Divided by 2 output:

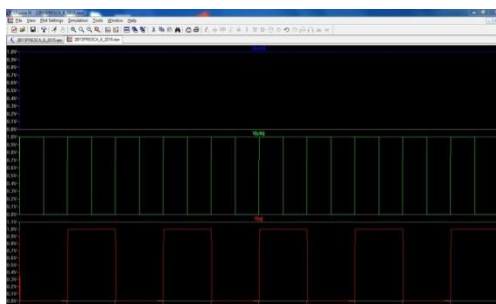


Fig. 5: divided by 2 wave form

Divided by 3 output:

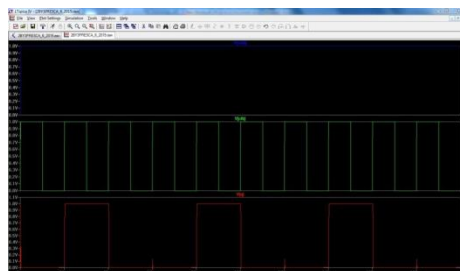


Fig. 6: divided by 3 wave form

II. Conclusion

This paper presents a 2/3 Prescaler (Programmable Frequency Divider) designed using a 45nm CMOS process, incorporating various D-flip-flop logic styles. Based on simulation results, it is observed that the 2/3 Prescaler implemented with Pass Transistor Logic (PTL) achieves very low power dissipation, while the design using transmission gates offers the highest speed, indicating significantly lower delay compared to other logic styles at a 1V supply in 45nm technology. The D flip-flop (DFF) in the prescaler is controlled by a mode control signal and is powered down during idle states. Additionally, the DFFs in the program counter and

swallow counter are shared, further reducing power consumption. Experimental results demonstrate a significant reduction in power usage, confirming that the proposed divider is highly suitable for low-power design applications.

Table –I Comparative Analysis of 2/3 Prescaler

S.NO	Parameters	2/3 Prescaler using with Different Logic					
1.	Design AND-OR GATE	AND-OR GATE using CMOS			AND-OR GATE using GDI Logic		
2.	Design D Flip-flop	TSPC	Transmission Gate	Pass Transistor	TSPC	Transmission Gate	Pass Transistor
3.	Used Technology	45nm	45nm	45nm	45nm	45nm	45nm
4.	Power Dissipation(in 2 Divided)	6.8648μW	9.1762μW	7.5287μW	12.259μW	8.8736μW	5.9257μW
5.	Power Dissipation(in 3 Divided)	6.7438μW	8.676μW	6.4414μW	4.7595μW	7.0981μW	4.5681μW
6.	Delay(in 2 Divided)	131.004ps	117.031ps	124.891ps	131.295ps	115.476ps	122.044ps
7.	Delay(in 3 Divided)	131.277ps	117.904ps	125.255ps	132.366ps	116.058ps	123.765ps

References

1. Badiali, Alessandro, and Mattia Borgarino. "Low-Power Silicon-Based Frequency Dividers: An Overview." *Electronics* 14.4 (2025): 652.
2. Deshpande, Yogita, and Yogita Vaidya. "Current Crafting: Mastering Low-Power Configuration Methods." 2023 International Conference on Next Generation Electronics (NEleX). IEEE, 2023.
3. Shaik Peerla, Rizwan, Ashudeb Dutta, and Bibhu Datta Sahoo. "An Extended Range Divider Technique for Multi-Band PLL." *Journal of Low Power Electronics and Applications* 13.3 (2023): 43.
4. Maity, Subhanil, and Sanjay Kumar Jana. "Design of a power-performance-area (PPA) optimized MOS current mode logic pre-scaler." *Circuits, Systems, and Signal Processing* 42.10 (2023): 5783-5798.
5. Daniels, Kyle. Low-Power, High-Performance Frequency Dividers for a Phase-Locked Loop. MS thesis. Auburn University, 2020.
6. Liao, Dongyi, et al. "An mm-wave synthesizer with robust locking reference-sampling PLL and wide-range injection-locked VCO." *IEEE Journal of Solid-State Circuits* 55.3 (2020): 536-546.
7. Bingham, Ned, and Rajit Manohar. "QDI constant-time counters." *IEEE Transactions on Very Large-Scale Integration (VLSI) Systems* 27.1 (2018): 83-91.
8. Gangasani, Gautam. Architectures and Circuits Leveraging Injection-Locked Oscillators for Ultra-Low Voltage Clock Synthesis and Reference-less Receivers for Dense Chip-to-Chip Communications. Diss. Columbia University, 2018.
9. Marković, Dejan. "2.3 Synthesis of CMOS Pass-Transistor Logic." *Digital Design and Fabrication* (2017): 39.
10. Bai, Yuxin, et al. "Architecting a MOS current mode logic (MCML) processor for fast, low noise and energy-efficient computing in the near-threshold regime." 2015 33rd IEEE International Conference on Computer Design (ICCD). IEEE, 2015.