

Low Power High Speed Multiplier Based on Spurious Power Suppression Techniue

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Abstract: A multiplier is one of the key hardware blocks in most digital and high performance systems such as FIR filters, digital signal processors and microprocessors etc. Multiplier is such an important element which contributes substantially to the total power consumption of the system. On VLSI level, the area also becomes quite important as more area means more system cost. Speed is a key parameter while designing a multiplier for a specific Application. These three parameters i.e. power, area and speed are always traded off. Speaking of DSP processors, area and speed are the most important factors. But sometimes, increasing speed also increases the power consumption, so there is an upper bound of speed for a given power criteria. Considering the battery operated portable multimedia devices, low power and fast designs of multipliers are more important than area. Generally as we know multiplication goes in two basic steps, Partial product and then addition. Hence in this paper we have first tried to design ripple carry adder and carry select adder and compare their speed and complexity of circuit i.e. the area occupied. While comparing the adders we found out that Ripple Carry Adder had a smaller area while having lesser speed, in contrast to which Carry Select Adders are high speed but posses a larger area. The result is a completely synthesized Efficient 8-by-8 shift and adds multiplier with low power and low area compared to the low power structure called bypass zero, feed a directly (BZ-FAD) TECHNIQUE of shift-and-add multipliers. The simulation result for 8 bit multipliers shows that the proposed low power architecture lowers the total power consumption by 51.11% when compared to the conventional architecture.

Keywords: Low power multiplier, Controller, Shift and Add multiplier, Partial Products, Sources of switching activities.

I. Introduction

Multipliers play an important role in today's digital signal processing and various other applications. With advances in technology, many researchers have tried and are trying to design multipliers which offer either of the following design targets – high speed, low power consumption, regularity of layout and hence less area or even combination of them in one multiplier thus making them suitable for various high speed, low power and compact VLSI implementation.

The common multiplication method is “add and shift” algorithm. In parallel multipliers number of partial products to be added is the main parameter that determines the performance of the multiplier. To reduce the number of partial products to be added, Modified Booth algorithm is one of the most popular algorithms. To achieve speed improvements Wallace Tree algorithm can be used to reduce the number of sequential adding stages. Further by combining both Modified Booth algorithm and Wallace Tree technique we can see advantage of both algorithms in one multiplier. However with increasing parallelism, the amount of shifts between the partial products and intermediate sums to be added will increase which may result in reduced speed, increase in silicon area due to irregularity of structure and also increased power consumption due to increase in interconnect resulting from complex routing. . On the other hand “serial-parallel” multipliers compromise speed to achieve better performance for area and power consumption. The selection of a parallel or serial multiplier actually depends on the nature of application. The power consumption in digital CMOS circuit is expressed as $p = I_{\text{standby}} V_{\text{dd}} + I_{\text{leakage}} V_{\text{dd}} + I_{\text{sc}} V_{\text{dd}} + \alpha C_L V_{\text{dd}}^2 f_{\text{clk}}$.

The standby current I_{standby} is the DC current drawn continuously from the power supply to ground. The leakage current I_{leakage} is, primarily determined by the fabrication technology, caused by the reverse bias currents in the parasitic diodes formed between source and drain. The short circuit current I_{sc} is the DC path between the supply rails during output transitions, the last term refers to the capacitive power dissipation with switching activity α , C_L the load capacitance at the output node, V_{dd} is the power supply voltage and f_{clk} is the clocking frequency. Shift-and-add multiplication is similar to the multiplication performed by paper and pencil. This method adds the multiplicand X to itself Y times, where Y denotes the multiplier. To multiply two numbers by paper and pencil, the algorithm is to take the digits of the multiplier one at a time from right to left, multiplying the multiplicand by a single digit of the multiplier and placing the intermediate product in the appropriate positions to the left of the earlier results. Many research efforts have been devoted for reducing the power dissipation of different multipliers (e.g., [1], [5], [6], [8], [9], and [11]). Among multipliers, tree multipliers are used in high speed applications such as filters, but these require large area. The carry-select-adder (CSA)-based radix multipliers, which have lower area overhead, employ a greater number of active transistors for the multiplication operation and hence consume more power. Among other multipliers, shift-and-add multipliers have been used in many applications for their simplicity and relatively small area requirement [3]. For SPST implementation we used the circuit details of [4]. In this work, we have used the ripple carry adder which has the least average transition per addition among the look ahead, carry skip, carry-select, and conditional sum adders [10].

The rest of the paper is organized as follows. Section II briefly reviews the background information about conventional shift and adds multiplier. Section III describes the architecture description of the proposed low power multiplier. Results are discussed in section IV and conclusion is in the last section.

II. Conventioinal Shift And Add Multiplier

The conventional shift-and-add multiplier architecture is shown in Fig. 1 [1], multiplies A by B. The major sources of switching activities of the multiplier are marked with dashed ovals and are as follows

- Shifts of the B register;
- Activity in the counter;
- Activity in the adder;
- Switching between “0” and A in the multiplexer;
- Activity in the mux select controlled by B (0);
- Shifts of the partial product register;

One should note that the activity of the adder consists of required transitions (when B (0) is non zero) and unnecessary transitions (when B (0) is zero). By minimizing or removing one or more of these switching activities results in lower power consumption.

Next, the proposed low power architectural description is as follows.

III. Proposed Low Power Architecture

To obtain low power architecture, we focus on eliminating or reducing the sources of switching activities shown in the previous section.

The motive is to design a shift-and-add multiplier.

Each of the modules of the proposed multiplier is explained as follows

A. Controller— It is the controlling part of the multiplier, takes a START signal and commands all initial modules until result is acquired and produces a STOP signal. Initially controller is in the idle state. It will enter in to the initial state after the start signal is set. If LSB=1, Add and Shift operations has been done and if LSB=0, shift operation will takes place directly. After reaching the maximum count, state machine reaches back to idle state and outputs the STOP signal. The finite state machine diagram is as shown in Fig. 2.

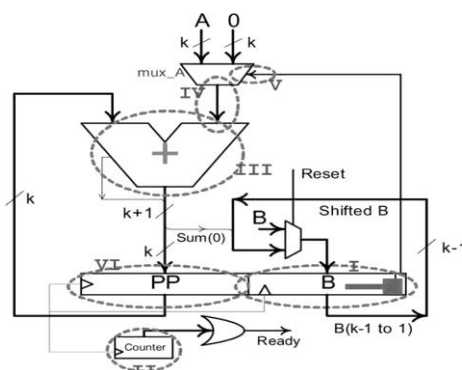


Fig. 1 Architecture of conventional shift-and-add multiplier with major sources of switching activities

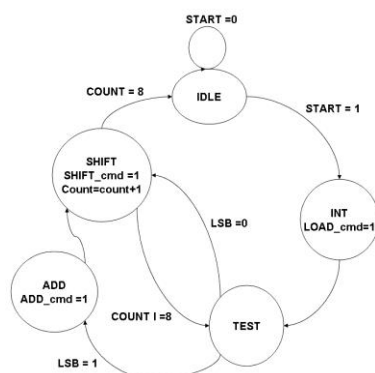


Fig. 2 Controller Diagram

B. *Multiplicand Block*— it is built up with D flip-flops, stores ‘A’ byte for processing, whenever the load_cmd is received from the controller. If LOAD_cmd=1, the flip-flops gets loaded and by applying the Reset, it clears the register. The structure of the multiplicand is as shown in Fig. 3.

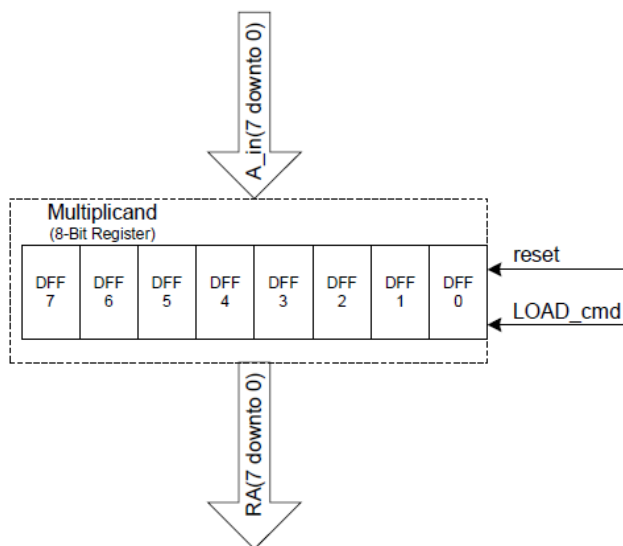


Fig. 3 Multiplicand Block

C. *Multiplier_Result block*— This Block stores the entire result and it is of 17 bits in size. It is build up with multiplexers and shift registers. The inputs to the block are Multiplier (B_in) and the outputs of the block are controller input, Adder input and the Multiplier_Result. At every stage, Controller input is fed back to the controller. Until the final result is obtained, Adder input is fed back to add up with the multiplicand. If LSB=0, SHIFT_cmd priors to ADD_cmd and the register shifts to right. If LSB=1, an ADD_cmd priors to SHIFT_cmd get loaded in to Multiplier_Register, bits 1 to 7 will be placed in to 0 to 6 positions of the register and the 9 adder bits will be placed in to bits 7 to 15 and then shifts the register bits. The block is as shown in Fig. 4.

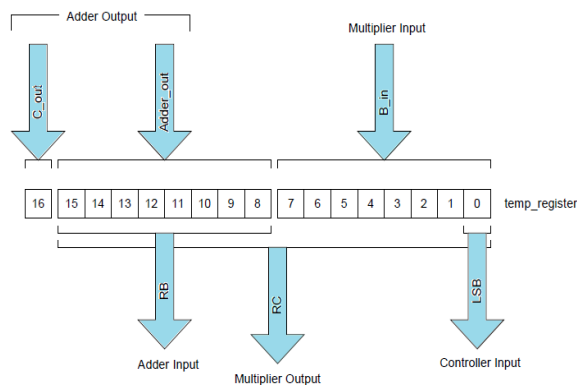


Fig. 4 Multiplier_Result Block

D. *Adder*— Adder is the most essential part of the multiplier to determine area and speed. These factors will be examined by the number of additions performed in the multiplication process. Adder will be designed using full adders. It consists of two inputs, carries in and produces a sum and carry out as the outputs. In this paper Ripple Carry Adder and Carry select Adder are compared.

In terms of area, Ripple Carry Adder is the best one. With respect to speed Carry Select Adder is the best choice. We designed the multiplier with Ripple Carry Adder. The compared values are shown in Table I.

Table I Comparson Of Adders

Adder Type	Synthesis	
	Critical Path Delay	Area(LUT)
Ripple Carry Adder (DFF behavioral)	15.761 ns	15
Carry Select Adder (DFF behavioral)	13.568 ns	20

E. *Multiplier*— the multiplier is designed by combining all the initial modules described in the previous sections and it is as shown in Fig. 5.

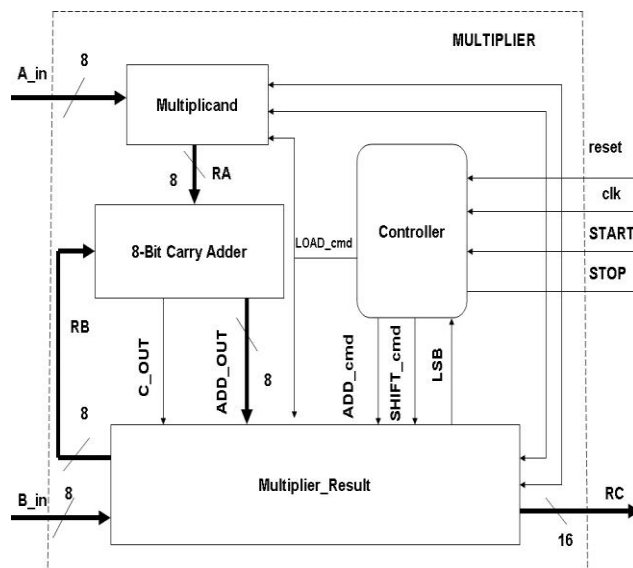


Fig. 5 Multiplier Block

IV. Results

In this paper we propose a low power and high speed shift and add multiplier. The proposed design of 8 bit multiplier can be verified using Modelsim 5.5 with VHDL code and it is shown in Fig. 6. The power consumption is Analyzed using Xilinx software (Spartan 3) and its reports are shown in Table. II and for conventional multiplier shown in [2] The Simulated delay report for 8-Bit Conventional multiplier is given in [2] and for proposed multiplier is as shown in Table. III the Power and Delay Comparison for Conventional and Proposed 8-Bit multiplier is as shown in Fig. 7.

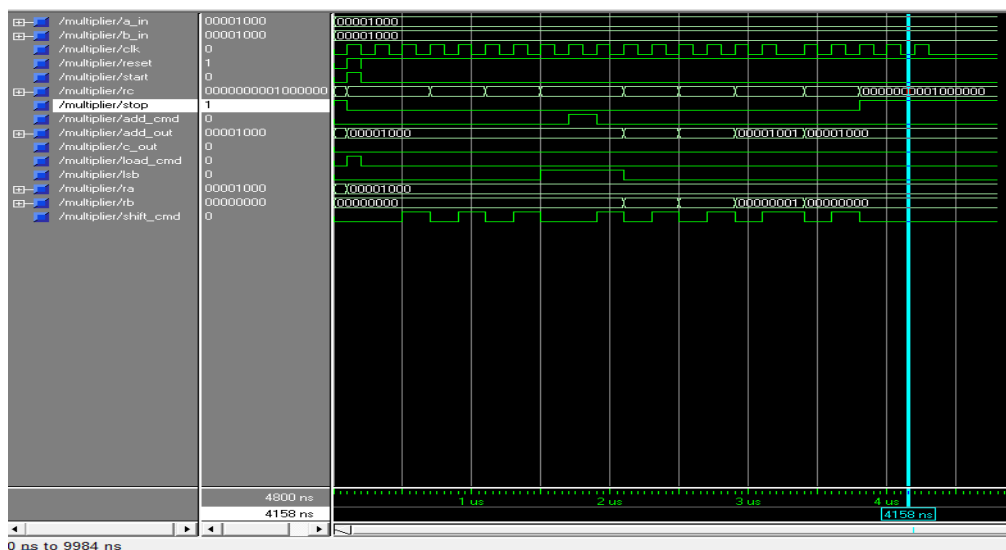


Fig.6 Simulation results for 8-bit using proposed architecture

Table II Power results for the proposed multiplier

	Volts	Degrees Centigrade	Milli Watts	Hours
$V_{cc INT}$	2.5			
Ambient temp		25		
Junction temp		28		

Quiescent power			56.37	
Battery Capacity(mA)				2850
Battery Life				96.45
Total power			73.87	

Table.III

Timing Summary
Minimum period: 4.849ns (Maximum Frequency: 206.232MHz)

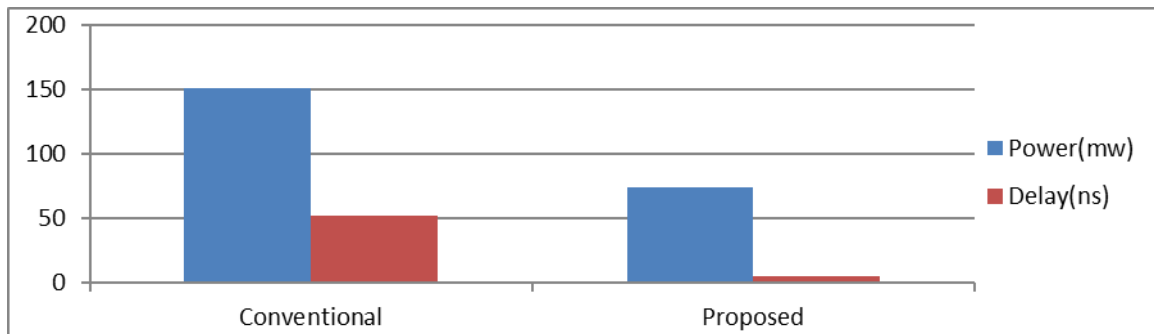


Fig. 7 Power and Delay Comparison for Conventional and Proposed 8-Bit multiplier

V. Conclusion

The proposed architecture lowers the power dissipation and Delay when compared to a conventional shift and add multiplier shown in Fig. 7. The simulation result for 8 bit multipliers shows that the proposed low power architecture lowers the total power consumption by 51.11% when compared to the conventional architecture.

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