

Concept Paper on Design and Optimization of Energyefficient Architectures for Edge Computing

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ABSTRACT

Edge computing is now transforming how data is processed by shifting the computing devices closer to the source of data generation. Even though this transformation helps reduce latency and bandwidth consumption, it introduces a critical challenge. The edge devices operate with strict hardware constraints. The conventional microcontrollers such as ATmega328p and ESP32 offer simple and reliable design while they come with lack of architectural mechanism for advanced energy optimization.

This research proposes the idea of designing an edge oriented, System on Chip (SoC) implemented using Verilog, integrating a 32bit Reduce Instruction Set Computing V(RISC-V/ RV32I) core with essential peripherals for the proposed microcontroller design. The new architecture explores energy minimization strategies including Dynamic Voltage and Frequency Scaling (DVFS), Sleep Modes, Clock Gating, Approximate ALU (Arithmetic and Logic Unit) in a separate manner. All the techniques will be implemented and evaluated separately. After thorough evaluation all techniques will be synergized and evaluated in one system. By means of Xilinx Vivado simulation and power analysis, a structured experimental matrix compares the baseline design against the optimized variants mentioned above. To represent edge workloads an integer multiplication (N32/64) and FIR (Finite Impulse Response) filtering will be compiled using RISC-V32 GCC toolchain under Ubuntu Operating System and executed on the soft SoC. The estimations of power, latency and Hardware areas such as LUTs (Look Up Tables), Registers, BRAM (Block Random Access Memory) will be measured and compared to evaluate energy, latency and area tradeoffs.

The study leverages recent research in energy efficient RISC-V microarchitectures, approximate computing and adaptive DVFS policies. This research contributes a reproducible methodology for architectural energy optimization in edge computing by providing a quantitative evaluation within a unified FPGA (Field Programmable Gate Array) based framework. The expected outcome is a demonstrable reduction in dynamic and static power while maintaining an acceptable performance degradation, setting up design guidelines for next generation energy-aware embedded architectures.

Keywords: Edge Computing, RISC-V, Energy Optimization, Clock Gating, DVFS

INTRODUCTION

During the past decade, computation and data processing have gradually shifted away from centralized cloud infrastructures towards distributed edge systems where data is processed near to the source of the data. The realworld applications such as environmental sensing, smart agriculture, industrial Internet of Things (IIoT), wearable health monitoring, and embedded robotics demand local data processing with minimal latency. Nevertheless, unlike cloud servers, edge devices operate under tight power and resource restrictions, often relying on batteries or energy harvesting. As a result, energy efficiency is no longer an optional optimization, it is now a key system design requirement.

The conventional widely used microcontrollers platforms were designed primarily for deterministic control applications. While they are highly reliable and easy to deploy, they lack combined architectural features such as optimized clock gating techniques suitable for edge computing, adaptive voltage scaling, or approximate arithmetic units. As edge workloads scale, these hardware limitations increasingly compromise system throughput and efficiency.

The emergence of the open RISC-V instruction set architecture has provided researchers with a flexible foundation for experimenting with custom microarchitectures [1]. Recent work has shown that tailored RISC-V cores can significantly improve energy efficiency through architectural modifications [2], [3]. Techniques such as clock gating reduce unnecessary switching activity, while Dynamic Voltage and Frequency Scaling (DVFS) exploits the quadratic dependence of dynamic power on supply voltage [4].

Dynamic power in Complementary Metal Oxide Semiconductor (CMOS) circuits is described by:

$$P_{dyn} = \alpha \cdot C \cdot V^2 \cdot F$$

where switching activity (α), capacitance (C), supply voltage (V), and operating frequency (F) determine power consumption. Reducing voltage yields substantial energy savings, especially in low-frequency edge workloads.

Approximate computing has also gained traction as a method for improving energy efficiency in error-tolerant applications such as signal filtering or matrix operations [5], [6]. Instead of computing with full precision, approximate arithmetic units intentionally reduce accuracy within acceptable margins to lower switching activity and hardware complexity.

Although each of these techniques has been studied independently, there is limited research evaluating them collectively within a unified microcontroller-style SoC. This study addresses that gap by designing a Verilogbased RISC-V SoC and systematically evaluating six architectural configurations under identical workloads. The goal is not merely to reduce power, but to understand the tradeoffs between energy, performance, and hardware cost in edge-oriented systems.

LITERATURE REVIEW

Energy-efficient processor design has been a dynamic field of research, particularly in the context of Internet of Things (IoT) and edge computing. Benini et al. [2] explored ultra low power RISC V cores operating near threshold voltage, demonstrating significant energy reductions for embedded workloads. In the same way, Palossi et al. [3] introduced adaptive RISC-V microcontrollers that dynamically adjust operating conditions based on workload intensity. Clock gating remains one of the most widely adopted power-saving techniques in both (Application Specific Integrated Circuit (ASIC) and Field Programmable Gate Arrays (FPGA) designs. By disabling clock signals to inactive modules, unnecessary switching activity is minimized [4]. In FPGA implementations, careful gating strategies have shown measurable reductions in dynamic power without major architectural changes.

DVFS continues to be a powerful mechanism for energy control. Since dynamic power scales with V^2 , voltage reduction produces substantial savings [7]. Recent research in 2025 integrates lightweight DVFS controllers within RISC-V systems for adaptive power management [8]. Approximate computing has gained renewed interest in edge systems. Han and Orshansky [5] demonstrated how reduced-precision arithmetic units can lower energy consumption in digital signal processing. More recent work extends these ideas to RISC-V cores with configurable precision levels [9]. Partial reconfiguration in FPGA-based systems provides another dimension of energy optimization, allowing unused modules to be dynamically disabled or replaced [10]. Regardless of these advances, most prior work evaluates individual techniques in isolation. Few studies present a complete, controlled comparison of multiple architectural energy-minimization strategies within a single embedded SoC.

This research contributes a structured experimental framework that evaluates baseline and optimized designs under consistent workloads and metrics.

METHODOLOGY

SoC Architecture Design

The proposed SoC design utilizes a streamlined, microcontroller centric architecture. This design prioritizes efficient execution and predictable hardware behavior, structured around the following core components of the microcontroller:

1. **RV32I RISC-V Processor Core:** When it comes to Instruction Set of the system is an in order RISC-V core, implemented in Verilog. By adopting the RV32I base integer instruction set, the core design of the device is engineered to minimize the amount of physical space it takes up, resulting in a smaller, more space efficient unit while maintaining compatibility with a modern, open-standard compiler toolchain.
2. **Integrated Memory Subsystem:** To facilitate low-latency access, the SoC follows the Harvard Architecture on which separate on chip instruction and data memories are implemented. These memory components are implemented using FPGA Block RAM (BRAM), providing high speed, single cycle data retrieval essential for real time edge processing.
3. **Essential I/O Peripherals:** A standard array of peripherals including (Universal Asynchronous Receiver and Transmitter) UART for serial communication, Analog to Digital Converter (ADC) , General Purpose Input/Output (GPIO) for digital interfacing, and a hardware Timer / Counter enables the SoC to interact seamlessly with external sensors and actuators.
4. **Clock and Power Management:** The architecture includes a dedicated clock management module to regulate system timing. For specialized, low power variants, an integrated power control unit manages energy distribution, allowing for more aggressive power saving strategies. The SoC logic supports DVFS, the FPGA implementation utilizes Frequency Scaling via clock dividers, while the Voltage Scaling component is modelled analytically using the V^2 relationship to estimate ASIC-level savings.

In its baseline configuration, the design emphasizes simplicity and stability, operating under a single global clock domain without active power gating or frequency scaling.

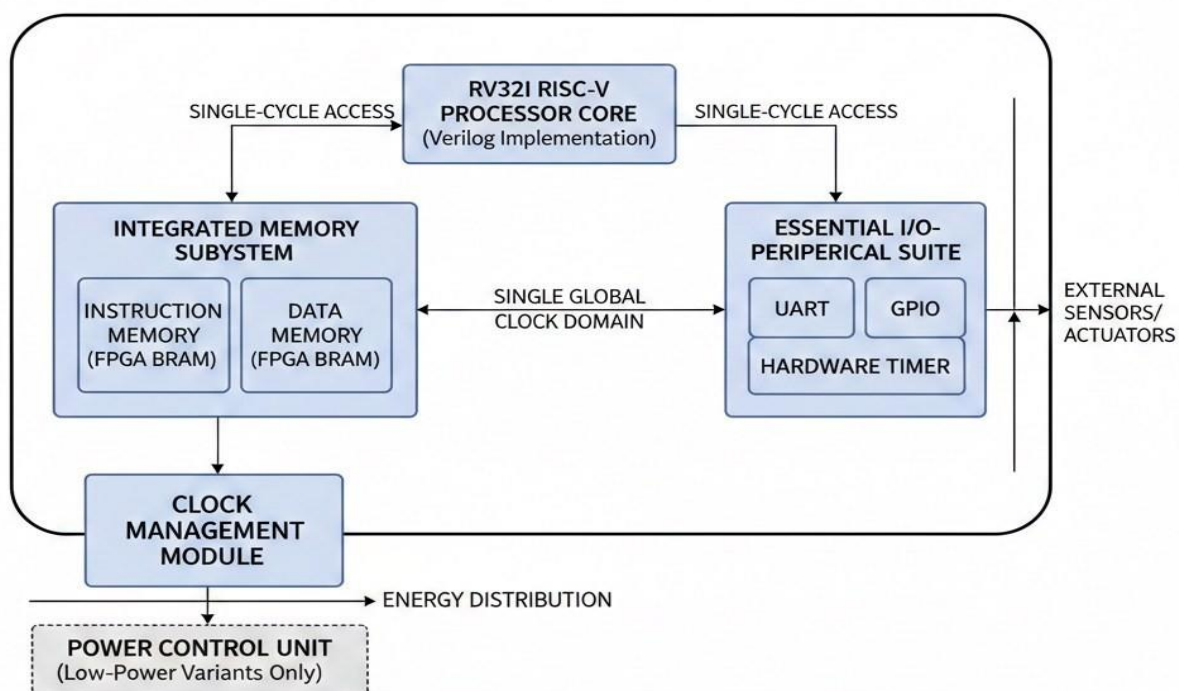


Figure 1: Typical SOC Architecture

The system is designed inspiring the Harvard Architecture, separating instruction and data paths to allow for parallel access. It illustrates a specialized 32-bit RISC-V processor environment tailored for executing precompiled hex files.

System Data Flow occurs with respect to the following machine cycle.

- **Instruction Fetch:** The PC sends an address to the Instruction Memory.
- **Decoding:** The fetched instruction is passed to the Decoder, which translates the 32-bit RISC-V command.
- **Execution:** The Decoder triggers the necessary Registers and ALU operations within the Core.
- **Data Access:** The CPU Core communicates with the Data Memory to read or write information as dictated by the program logic.

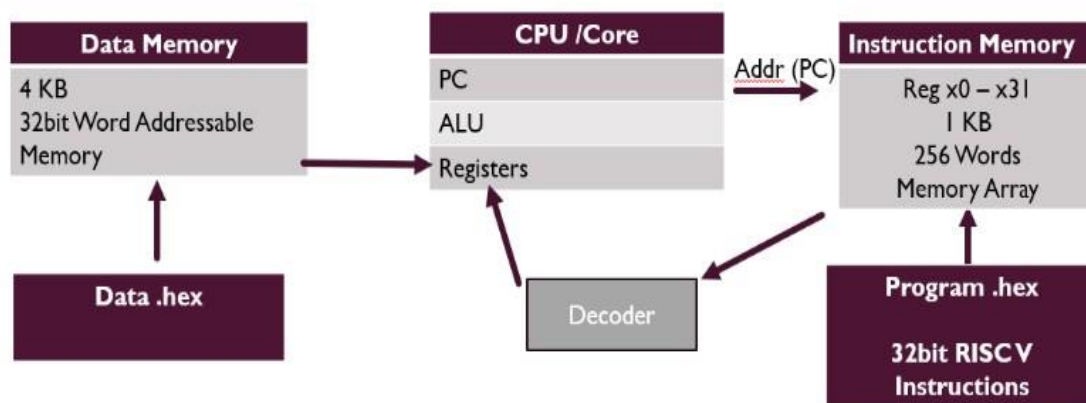


Figure 2: System Data Flow

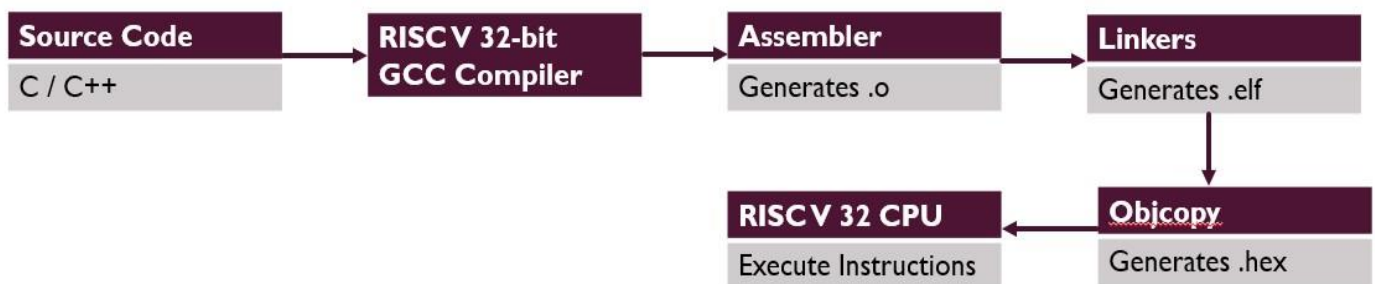


Figure 3: RISC-V Instruction Generation and Execution

Experimental Configuration

To evaluate the efficiency and flexibility of the proposed RV32I SoC, the design will be deployed across six distinct architectural configurations. Each configuration targets a specific balance between computational throughput and energy economy.

Baseline (With no Optimization)

The Baseline configuration serves as the control group for all subsequent benchmarks. In this mode, the entire SoC operates under a single, continuous global clock domain. There is no logic to disable inactive modules, and

the ALU always maintains full 32-bit precision. This setup represents the maximum power consumption profile but provides the most stable and predictable timing for real time applications.

Clock Gating Only

This configuration enables detailed fine level management of clock gating at the Register Transfer Level (RTL). By means of integrated clock gating (ICG) cells, the system dynamically shuts off the clock signal to functional blocks such as the UART, Timer, or specific Register File ports whenever they are not actively processing data. This reduces dynamic power dissipation by minimizing the switching activity of the internal nodes.

Sleep Modes Only

In this design variant, the SoC implements a stratified Power Management State Machine. The system core can engage a Deep Sleep or Idle state during periods of inactivity (e.g., waiting for an external GPIO interrupt). While the memory subsystem remains powered to retain state, the RISC-V pipeline is effectively frozen. This is particularly effective for edge sensing applications that spend the majority of their operational life in a "listen" mode.

Approximate ALU Only

The Approximate ALU configuration explores the trade-off between mathematical accuracy and hardware resources. Instead of computing with full precision, this design intentionally reduces accuracy within acceptable margins to lower switching activity and hardware complexity. Specifically, this architecture replaces the standard 32-bit integer units with the following:

- **Multiplier Truncation:** The multiplier employs a Static Segment Method (SSM), where the lower 12 bits of the partial products are truncated before summation. This significantly reduces the number of full adders in the multiplier tree.
- **LSB Masking:** The adder utilizes a Lower-Part OR Adder (LOA) logic. In this approach, the 8 least significant bits (LSBs) are computed using a bitwise OR operation, eliminating the carry-propagation chain for those bits.
- **Targeted Workloads:** This optimization is applied to error-tolerant tasks like the 32-tap FIR Filter. By prioritizing high-order bit precision, the design reduces the critical path and logic gates (LUTs) while maintaining a performance degradation of less than 10%

Simulated DVFS (Dynamic Voltage and Frequency Scaling)

This mode simulates the effects of DVFS by defining three specific operating points (P-states). The system can transition between:

- **High Performance:** Maximum frequency and nominal voltage.
- **Balanced:** Medium frequency for steady-state processing.
- **Eco:** Minimum frequency and reduced voltage for background tasks. By scaling the frequency (f) and voltage (V) together, the power savings follow a cubic relationship, offering the most drastic reductions in energy consumption for varying workloads.

Combined Policy (Adaptive Power Controller)

The final configuration is a sophisticated, featuring an Integrated Adaptive Power Controller. This unit acts as a hardware orchestrator, monitoring the instruction stream and peripheral demand in real time. It intelligently combines the previously mentioned techniques into a single cohesive policy. It ensures that

the SoC only draws the exact amount of power required for the immediate task, representing the philosophy of "lean execution".

Benchmark

To evaluate the effectiveness of the power saving strategies implemented and the architectural efficiency of the SoC, a meticulous benchmarking methodology is employed. This process involves executing specific real world workloads and capturing hardware level metrics to quantify the trade offs between performance and energy consumption.

Workload Selection

The benchmarks consist of two representative kernels that reflect the demands of modern edge computing:

1. Integer Matrix Multiplication (N=32, 64): This workload serves as an agent for compute-intensive workloads, such as those found in neural network layers or coordinate transformations. By scaling the matrix size from 32×32 to 64×64 , the system's ability to handle increasing computational complexity and memory access patterns is assessed.
2. 32-tap FIR Filter: Representing a Digital Signal Processing (DSP) workload, this benchmark involves continuous multiply accumulate (MAC) operations. It simulates real time data streaming scenarios common in sensor fusion and audio processing at the edge.

Compilation and Loading Process

The software environment is regulated to ensure results are comparable across all hardware configurations.

- The high level programs (C/C++) are compiled using the RISC-V32 GCC toolchain within an Ubuntu environment.
- The generated code after the compilation conforms to the RV32I base integer instruction set. The all generated machine instructions belong exclusively to the standard 32-bit integer operations defined within the base RISC-V ISA.
- The resulting binary files are converted into .hex files, which are then loaded into the instruction memory by simulating a typical embedded firmware boot sequence.

Evaluation Metrics

To provide a holistic view of the SoC's efficiency, data is collected across three primary categories:

Table 1: Evaluation Metrics

Metric	Description
Total Energy (Joules)	The cumulative power consumed over the duration of the workload, capturing the impact of both static leakage and dynamic switching.
Cycles per Workload	A measure of execution time and throughput, identifying any performance overhead introduced by power management logic
Resource Utilization	The hardware cost in terms of LUTs (Look-Up Tables), Registers, and BRAM blocks used on the FPGA for each configuration.

Preliminary Results

To establish a reference point for the proposed energy-efficient variants, a baseline simulation of the RV32I SoC was conducted using the Xilinx Vivado environment. The primary objective was to validate the functional correctness of the instruction decoder and the execution pipeline under standard workloads.

The core was tested using a sequence of immediate arithmetic instructions compiled via the RISC-V32 GCC toolchain. As shown in Table 2, the hex-to-assembly mapping confirms that the SoC correctly translates and executes the 32-bit RISC-V commands. This confirms the hardware's compatibility with the standard RV32I ISA.

Table 2: A piece of the sample instructions loaded to the Instruction Memory

Hex Code	Assembly Instruction	Description
00200093	addi x1, x0, 2	x1 = 2
00300113	addi x2, x0, 3	x2 = 3
00400193	addi x3, x0, 4	x3 = 4
00500213	addi x4, x0, 5	x4 = 5
00600293	addi x5, x0, 6	x5 = 6
00700313	addi x6, x0, 7	x6 = 7
00800393	addi x7, x0, 8	x7 = 8

The execution of a 30-instruction test kernel provided the first quantitative performance data for the architecture. The simulation metrics extracted from the Vivado Tcl Console (see Figure 4) reveal the following baseline characteristics:

- Cycles per Instruction (CPI): The system achieved a CPI of 1.033, indicating high efficiency in the single-cycle execution of integer operations.
- Execution Latency: The average instruction latency was measured at 10.33 ns, providing a timing foundation for real-time edge processing requirements.
- Throughput: The total execution of 30 instructions was completed in 31 cycles, validating the predictable hardware behaviour of the Harvard-based memory subsystem.

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===== Simulation Metrics =====
Total Cycles Executed : 31
Total Instructions    : 30
CPI                   : 1.033333
Average Instruction Latency (ns): 10.333333
=====

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Figure 4: Performance Metrics for the Baseline SOC

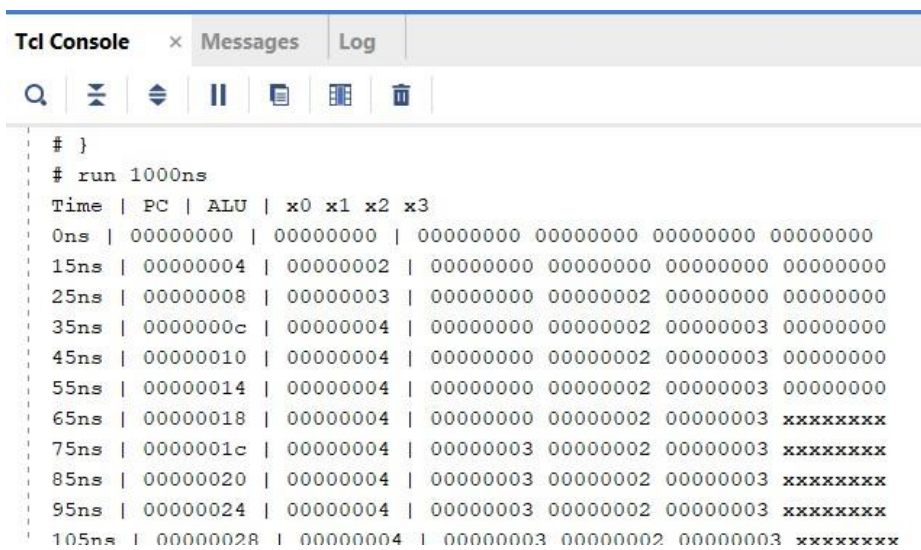


Figure 5: Functional Verification Waveform Log for RISC-V Register State Transitions

Significance

This research provides a systematic and practical evaluation of energy-efficient architectural techniques within a unified SoC framework. Instead of analyzing isolated optimizations, it quantifies how multiple strategies interact under realistic workloads.

The expected contributions include:

- Empirical Power Analysis:
 - Clear measurement of switching activity reduction through Integrated Clock Gating (ICG) cells.
- Mathematical Validation:
 - Validation of quadratic energy savings from DVFS based on the dynamic power formulation.
- Accuracy-Power Tradeoffs:
 - Quantification of precision–energy tradeoffs by implementing specific hardware truncations (e.g., LSB masking) in approximate arithmetic units.
- Hardware Overhead:
 - Detailed area analysis of the hardware cost in terms of LUTs, Registers, and BRAM blocks for each power-management variant.
- Policy Synergy:
 - Demonstration of the combined optimization synergy achieved by the Integrated Adaptive Power Controller.

Preliminary expectations suggest:

- Baseline Performance:
 - Functional validation of the RV32I core with a measured CPI of 1.033 and instruction latency of 10.33 ns in a simulated environment.

- Switching Efficiency:
 - A 20–40% dynamic power reduction through RTL-level clock gating.
- Error-Tolerant Savings:
 - An acceptable performance degradation of less than 10% for approximate FIR filtering while significantly reducing the multiplier's critical path.
- Optimized Energy-per-Operation:
 - Achievement of the best energy-per-operation profile under the adaptive "lean execution" combined policy.

While this study utilizes an FPGA-based framework for reproducible methodology, the RTL is designed for high-portability to ASIC (Application-Specific Integrated Circuit) manufacturing. Transitioning to a dedicated silicon process (e.g., 65nm CMOS) would allow for the physical implementation of True Voltage Scaling and the use of Multi-Threshold CMOS (MTCMOS) to further minimize leakage in sleep modes. This roadmap ensures the findings provide a verified foundation for next-generation, mass-produced energy-aware embedded processors.

CONCLUSION

This research presents the design and optimization of a Verilog-based RISC-V SoC tailored for energyconstrained edge computing environments. By systematically evaluating a suite of architectural strategies including RTL-level clock gating, stratified sleep modes, approximate arithmetic units, and simulated DVFS this study quantifies the critical tradeoffs between energy consumption, execution latency, and hardware area.

Preliminary experimental results from Xilinx Vivado simulations validate the functional integrity of the baseline RV32I core, demonstrating a stable CPI of 1.033 and an average instruction latency of 10.33 ns. The implementation of approximate computing through 12-bit multiplier truncation and 8-bit LSB masking in the ALU provides a pathway for significant power reduction in error-tolerant workloads, such as FIR filtering, with a performance degradation of less than 10%. Furthermore, the introduction of an Integrated Adaptive Power Controller demonstrates that a synergized "lean execution" policy can yield superior energy efficiency compared to isolated optimizations.

While this framework provides a reproducible FPGA-based methodology, it also serves as a verified foundation for future ASIC implementation, where true voltage scaling and multi-threshold CMOS techniques can be fully realized. Ultimately, the outcomes of this research offer actionable design insights for the development of nextgeneration, low-power embedded architectures, bridging the gap between high-performance processing and the stringent energy requirements of the intelligent edge.

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