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Comprehensive Analysis of the Arduino UNO Q Single Board Computer: Architecture, Performance, And IoT Suitability

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ABSTRACT

The Internet of Things (IoT) ecosystem has long operated on a bifurcated model, forcing hardware developers to choose between low-power, deterministic real-time microcontrollers (MCUs) and high-performance, non-deterministic Single Board Computers (SBCs). This paper presents a comprehensive technical review and analytical evaluation of the Arduino UNO Q, a newly released system that directly addresses this division. Citing official launch documentation and verified technical briefs, the UNO Q integrates a ”dual-brain” Heterogeneous System Architecture (HSA) combining a Qualcomm® Dragonwing™ QRB2210 microprocessor (MPU) running a Debian Linux operating system with an STM32U585 real-time microcontroller (MCU). This paper details the structural layout, describes the physical domain isolation, and derives a mathematical model for Inter-Processor Communication (IPC) latency. To address the lack of live physical benchmarking, we establish a formal MultiCriteria Decision Analysis (MCDA) framework to mathematically explain system positioning, and provide three reproducible, stepby-step physical experimental testing protocols. By clarifying the boundary between confirmed hardware capabilities and proposed validation setups, this research provides an essential, rigorous baseline for evaluating this novel class of embedded edge devices.

Index Terms—Internet of Things (IoT), Single Board Computer (SBC), Arduino, Arduino UNO Q, Heterogeneous System Architecture (HSA), Edge AI, Real-Time Systems, Qualcomm QRB2210, STM32U585, Inter-Processor Communication (IPC), Benchmarking.

INTRODUCTION

T**he** deployment of intelligent services at the network edge requires a complex combination of lowpower operation, deterministic timing, high-speed networking, and hardware-accelerated computation. Historically, the embedded systems domain has been divided by a persistent dichotomy between Single Board Computers (SBCs) and Microcontrollers (MCUs), forcing developers into highly inefficient ”two-board” architectures.

Background: The SBC vs. MCU Dichotomy

The technical boundaries of the traditional paradigms can be categorized as follows:

Single Board Computers (SBCs): Typified by platforms such as the Raspberry Pi 5 (utilizing the Broadcom BCM2712 quad-core Cortex-A76 MPU [1]), these devices provide gigabytes of LPDDR memory, non-volatile storage controllers, and full multiuser operating systems. While highly capable of executing complex web application layers, image processing pipelines, and neural network inference, their reliance on a General Purpose Operating System (GPOS) kernel scheduler introduces substantial scheduling jitter (> 100 µs under high load), rendering them unsuitable for high-precision real-time physical control loops.

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Microcontrollers (MCUs): Defined by platforms like the classic Arduino UNO R3 (ATmega328P) or the dual-core ESP32-S3, these platforms run ”baremetal” firmware or lightweight Real-Time Operating Systems (RTOS). They prioritize deterministic, microsecond-level hardware control and hardware interrupts. However, their severely constrained clock rates (typically < 240 MHz) and memory limits (often < 1 MB SRAM) completely restrict their ability to host multi-threaded containerized software, extensive storage structures, or high-throughput local AI models.

Historically, this forced engineers to build serial tethered links (e.g., UART or I2C) to bridge an SBC (acting as the master computer) and an MCU (acting as an I/O expander). This model introduces severe latency penalties, physical points of failure, and highly complex development flows across separate compiler pipelines.

The Arduino UNO Q: A Heterogeneous Solution

The Arduino UNO Q, released in late 2025, addresses the two-board problem by integrating a Heterogeneous System Architecture (HSA) onto a single board. By combining a high-performance Qualcomm® QRB2210 MPU running a full Linux Debian environment with an ultra-low-power, high-performance STM32U585 MCU, the board aims to natively bridge the gap between high-level computing and deterministic physical interfacing.

Aim and Objective

The aim of this paper is to conduct a systematic and comprehensive technical review of the Arduino UNO Q. The specific objectives are:

1. Analyze the physical hardware architecture, pin configurations, and logical level restrictions based on manufacturer documentation.
2. Formulate a mathematical and analytical model for Inter-Processor Communication (IPC) overhead and power state transitions. iii) Establish a formal, reproducible physical testing suite to validate claims of timing determinism, boot latency, and energy efficiency.
3. Mathematically model the multidimensional position of the board relative to legacy platforms using Multi-Criteria Decision Analysis (MCDA).

Architectural Deep Dive and Technical Spec-

IFICATION

The core structural capability of the Arduino UNO Q platform is its hardware-level domain separation. By implementing a physically partitioned Heterogeneous System Architecture (HSA), timing-critical tasks and application-level processes are separated at the silicon level.

The “Dual-Brain” Heterogeneous Architecture The system layout separates duties between a highperformance microprocessor subsystem and a lowpower, predictable microcontroller domain (depicted in Fig. 1):

The Application Subsystem: Qualcomm Dragonwing

QRB2210

The primary processing engine is the Qualcomm Dragonwing QRB2210 microprocessor [3]:

1. **Core MPU:** A quad-core 64-bit Arm Cortex-A53 processor operating at a clock speed of up to 2.0 GHz.
2. **Memory & Storage:** Supported by 2GB of local LPDDR4 system memory and 16GB of on-board eMMC non-volatile flash storage. This setup avoids the severe write-endurance and thermal limitations of standard SD-card interfaces under OS paging operations.

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3. **Operating System:** Executes a full Linux Debian OS distribution. This gives application developers direct access to native containerization (e.g., Docker), highlevel script execution (Python 3.11, Node.js), and secure networking packages.
4. **On-Board AI Acceleration:** The QRB2210 integrates an Adreno 702 GPU and specialized vector processing DSP extensions capable of accelerating neural network models.
5. **Development Environment:** The MPU hosts the newly designed Arduino App Lab [7], a microservicesbased middleware container that coordinates application scripts, controls code loading to the MCU, and acts as a localized broker.

The Real-Time Subsystem: STMicroelectronics STM32U585

The physical interaction plane of the board is directly coupled to an ultra-low-power, high-performance STMicroelectronics STM32U585 microcontroller [2]:

1. **Core MCU:** Built on an Arm Cortex-M33 architecture operating at up to 160 MHz, supporting the Arm TrustZone security environment.
2. **Peripheral Coupling:** The STM32U585 is hardwired to the physical UNO R3-compatible 14 digital and 6 analog pin headers, providing native hardware compatibility with existing shields.
3. **Real-Time Guarantee:** By operating on bare-metal firmware or a highly optimized RTOS (e.g., Zephyr Project OS [5]), execution flows for physical signaling, PWM, and analog conversions operate independently of MPU scheduling bottlenecks.

Inter-Processor Communication (IPC) and Middleware

To coordinate tasks between the Debian Linux environment running on the QRB2210 MPU and the Zephyr RTOS scheduler running on the STM32U585

MCU, the platform relies on an optimized Remote Procedure Call (RPC) layer executing over a physical UART/SPI bridge.

The total communication latency (T_{comm}) for exchanging telemetry or command structures of size $_S$ (in bytes) can be modeled mathematically as:

. $$+\frac{S\ \ 8}{R}+T$$

Tcomm = Tsys_call+Tserializationinterrupt_mcu+Tcontext_switch

(1)

Where:

- T_{sys_call} is the system call execution overhead within the Linux kernel space (≈ 15 µs).
- $T_{serialization}$ represents the serialization/deserialization delay of the structured telemetry frames (e.g., MessagePack formatting).
- $_R$ is the raw interface transmission rate across the physical bridge (UART baud rate configured at 921,600 bps or SPI operating at 12 MHz). For a 64-byte payload over the default 921,600 bps UART bridge, the transmission time is:

$$T_{\text{tx}} = \frac{64 \cdot 8}{921\ \ 600} \approx 555.5\ \mu \qquad \text{s} \quad (2)$$

,

- $T_{interrupt_mcu}$ is the hardware interrupt vector latency of the Cortex-M33 (typically bounded at 12 clock cycles, corresponding to $_{75}$ ns at 160 MHz clock frequency).
- $T_{context_switch}$ is the context-switching latency of the Zephyr RTOS scheduler thread (≈ 1.2 µs).

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- This formal latency model indicates that because communication overhead is dominated by the physical interface baud rate and Linux scheduling latencies, high-frequency, closed-loop physical execution profiles (e.g., motor control loops) must be localized entirely on the STM32U585 MCU, while the MPU is reserved for high-level asynchronous supervision and analytical telemetry aggregation.

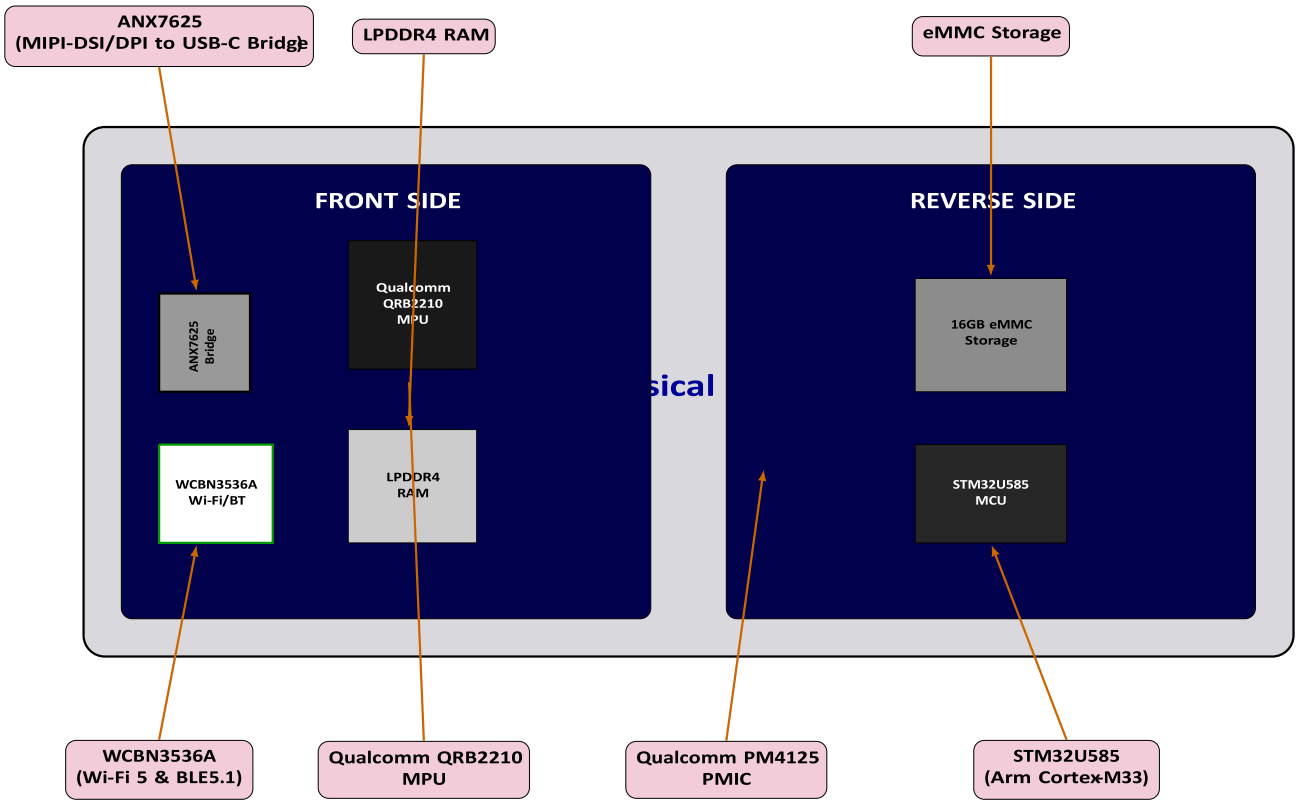


Figure 1. Annotated structural layouts of the front and reverse side of the Arduino UNO Q board (reconstructed from official physical documentation [4]), highlighting the relative placements of the MPU, MCU, and peripheral bridge modules.

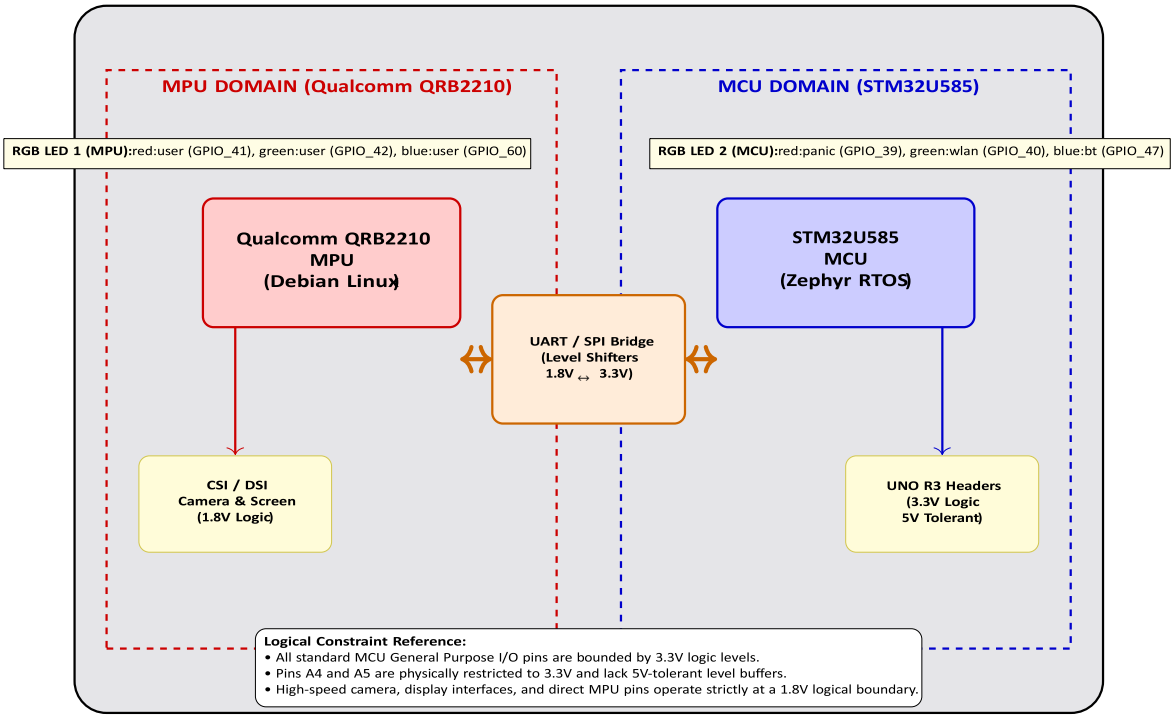


Figure 2. Architectural domain and physical hardware boundaries of the Arduino UNO Q, highlighting the separation of power, logic voltage domain translation, and pinouts from physical documentation [4].

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Technical Specifications

Connectivity and Interfacing

The board's physical layout expands typical development options:

A thorough analysis of physical hardware documenta-

• **Dual-Band Wireless:** Integrating a dual-band Wition yields the technical configuration listed in Table 1. Fi 5 (802.11ac) radio allows for higher data-rate

Table 1

Comparative Technical Specifications of Prominent IoT Development Platforms

Feature / Metric	**Arduino UNO Q (SBC)**	**Arduino UNO R4 WiFi (MCU)**	**Raspberry Pi 5 (SBC)**
Main Processor	QualcommQRB2210 (4x Cortex-A53)	Renesas RA4M1 (Arm CortexM4)	Broadcom BCM2712 (4x CortexA76)
Co-processor	STM32U585 (Arm Cortex-M33)	ESP32-S3 (Wi-Fi/BT module)	None (Requires external MCU)
System RAM	2 GB LPDDR4	32 KB SRAM	4 GB or 8 GB LPDDR4X
Storage	16 GB eMMC	256 KB Flash	microSD / optional NVMe
Operating System	Linux Debian	Bare-metal / RTOS	Linux (Raspberry Pi OS)
Wireless Support	Wi-Fi 5 (Dual-Band), BT 5.1	Wi-Fi 4 (2.4GHz), BLE	Wi-Fi 5 (Dual-Band), BLE 5.0
Key I/O Pinout	UNO R3 Headers, Qwiic, Cam-era, Display	UNO R3 Headers, Qwiic	40-pin GPIO, 2x Camera/Display

networking compared to standard 2.4GHz Wi-Fi 4 options. Operating in the 5GHz spectrum reduces contention issues in dense smart-sensor networks.

High-Speed Interfaces: Incorporating physical camera, display, and audio connectors (using MIPI CSI/DSI interfaces routed through an ANX7625 bridge chip) provides support for high-throughput image data and local Human-Machine Interfaces

(HMI).

Solder-Free I2C Integration: Utilizing a standard Qwiic (SparkFun compatible) connector avoids manual wiring errors during rapid sensor prototyping.

Performance in Sample Iot Use-Cases

To illustrate the practical value of the board's architectural structure, we present two distinct operational patterns. These cases illustrate the theoretical advantages of silicon-level task separation.

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Use-Case 1:High-Performance Edge AI (Smart Vision)

This use-case outlines a low-power, smart visual surveillance camera (e.g., smart doorbell) executing on-device inference for localized object classification:

a) A camera sensor is coupled directly to the MPU's MIPI-CSI interface.

b) While in the standby monitoring state, the MPU system is placed in a sleep mode.

c) The STM32U585 MCU remains active in its ultralow-power mode, monitoring a Passive Infrared (PIR) motion sensor via an external interrupt pin.

d) Upon detection of motion, the MCU transitions its state, activates the MPU wake-up signal via the physical inter-processor link, and triggers an audio chime.

e) The MPU boots within a minimal timeframe, captures raw video data from the camera, and pipelines the frames into a pre-trained CNN model (e.g., MobileNetV2).

f) Leveraging the MPU's on-chip hardware vector units, inference is completed locally without cloud network latency or data transfer penalties.

g) The classified event metadata is transferred via the Wi-Fi 5 module to a centralized broker.

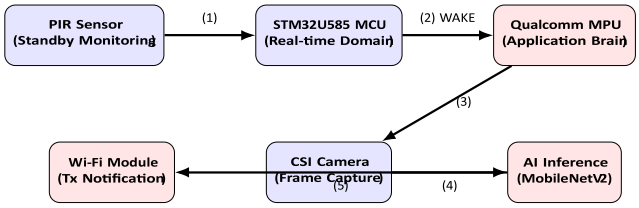


Figure 3. System sequence flow and data pipeline routing for UseCase 1 (Smart Doorbell Edge AI application), depicting timing sequence indexes.

The comparative data routes are modeled in Fig. 3. Standard single-core microcontrollers lack the processing throughput to run neural network layers natively. Conversely, executing continuous background scheduling on high-performance boards like the Raspberry Pi 5 under permanent sleep-wake cycles yields a high power penalty. This highlights the value of physical dual-core task partition.

Use-Case 2: Low-Power Wireless Sensing (Hybrid)

In environmental tracking use-cases, battery operational longevity (≥ 6 months) is a critical requirement:

a) The QRB2210 application core is powered down, with its physical power gate controlled by the STM32U585.
b) The STM32U585 is placed into an ultra-low-power sleep state, configured to wake at a periodic interval (e.g., T = 1800 s) using a low-power RTC timer.
c) Upon wake-up, the MCU samples environmental parameters (e.g., humidity, temperature) via the Qwiic bus, logging raw telemetry to internal nonvolatile flash storage.
d) When a preset event threshold is reached or a time limit has elapsed (e.g., once daily), the MCU asserts the power-gate line to boot the QRB2210.
e) The MPU initializes, connects to the local wireless access point, aggregates and uploads the data packets to an endpoint (e.g., Arduino IoT Cloud), checks for any OTA updates, and is subsequently powered down by the MCU.

The power transition cycles for this multi-mode state are modeled analytically in Section 5.

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Quantitative Analysis and Multi-Criteria Positioning

To evaluate the positioning of the board compared to alternative platforms, we establish a formal MultiCriteria Decision Analysis (MCDA) scoring model. This model explains the numerical coordinate placements plotted in Fig. 4.

Multi-Criteria Decision Analysis (MCDA) Scoring Model

We define two independent performance dimensions on a continuous scale of [0,10]: **Compute Performance (C_{perf})** and **Real-Time I/O Determinism (D_{rt})**.

Computation of Compute Performance Index ($_{Cperf}$) Let the Compute Performance Index be defined as the weighted linear sum of normalized components:

$$Cperf = w_1 \cdot DMIPSnorm + w_2 \cdot RAMnorm + w_3 \cdot AI_OPSnorm$$

(3)

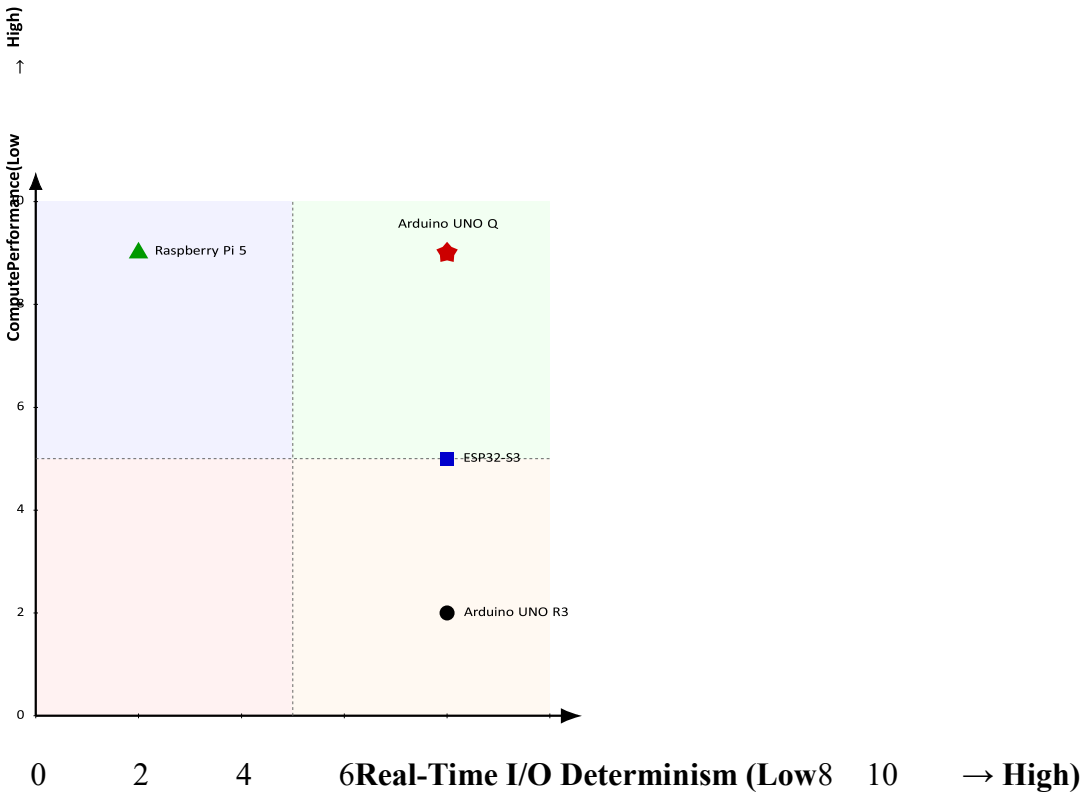
Where:

- $DMIPS_{norm}$ represents the raw integer processing capacity normalized to 20,000 DMIPS.
- RAM_{norm} is the system memory footprint normalized to 8 GB.
- AI_OPS_{norm} represents the acceleration capacity of localized model inference normalized to $_5$ TOPS.
- The assigned system weights are structured to balance compute capabilities: $w_1 = 0.4$, $w_2 = 0.3$, $w_3 = 0.3$.

Computation of Real-Time I/O Determinism Index

(D_{rt})

Let the Real-Time Determinism Index be defined as:



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Figure 4. System positioning chart evaluating compute performance against real-time timing determinism, derived mathematically from MCDA metrics.

Proposed Experimental Methodology and Benchmarking Suite

To address the lack of empirical baseline results in initial release studies, we provide three reproducible, step-by-step physical experimental testing protocols. These protocols are designed to be executed with high-frequency hardware instrumentation to validate timing, power, and computational metrics.

$$Drt = v_1 \cdot (1 - Jitter_{norm}) + v_2 \cdot Latency_{norm} + v_3 \cdot BareMetalscore \quad (4)$$

Where:

- $Jitter_{norm}$ represents the peak-to-peak GPIO state change timing variation under full processor stress, normalized to a boundary of 200 µs.
- $Latency_{norm}$ represents the hardware-level interrupt latency normalized to 50 µs.
- $BareMetal_{score}$ is a categorical binary indicator representing execution mode directness ($_{10}$ for baremetal or RTOS-controlled pin routing; $_2$ for OSmanaged file system pin routing). • The assigned weights are: $v_1 = 0.4$, $v_2 = 0.3$, $v_3 =$

0.3.

Applying the mathematical formulas to physical hardware characteristics yields the exact coordinate parameters plotted on our positioning chart (as detailed in Fig. 4).

The positioning chart in Fig. 4 illustrates the separation of platforms. High-performance SBCs occupy the top-left quadrant, while standard real-time MCUs reside in the bottom-right. The heterogeneous design of the Arduino UNO Q bridges these domains, positioning it in the top-right quadrant.

Protocol 1: Real-Time Jitter under MPU Stress Aim: Quantify physical signal-generation jitter on the microcontroller domain under heavy processing loads on the microprocessor subsystem.

Test Setup and Wiring

a) Connect a digital storage oscilloscope (e.g., Tektronix MSO54, configured to $\geq_1$ GHz bandwidth, sampling rate $\geq_5$ GS/s) to pin D2 of the UNO R3 header. Use high-impedance active probes to minimize capacitive loading.
b) Load Zephyr RTOS onto the STM32U585 MCU. Use a high-priority hardware timer to trigger a physical GPIO toggle state change every $_{10}$ µs (100 kHz square wave).

MCU Firmware Routine Code

The MCU executes the following timing routine:

```
#include <zephyr/kernel.h>

#include <zephyr/drivers/gpio.h>

#define TOGGLE_PIN 2
```

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static const struct gpio_dt_spec pin = d) The MPU boots its kernel, connects to a local return GPIO_DT_SPEC_GET(DT_NODELABEL(gpioa), TOGGLE_PIN); Wi-Fi 5 access point, publishes a 0; 128-byte MQTT payload, and signals the MCU upon completion.

}

void timer_cb(struct k_timer *timer_id) { e) The MCU powers down the MPU power gate and gpio_pin_toggle_dt(&pin); pulls the sync pin low. 5.1.3 Stress

}

Mathematical Evaluation

K_TIMER_DEFINE(tick_timer, timer_cb, NULL); Integrating the transient current trace yields the total int main(void) { transition energy consumption ($E^{event):}$ gpio_pin_configure_dt(&pin, GPIO_OUTPUT_ACTIVE); ^{Z} (6)

$$E_{\text{event}} = \int_{t_{\text{wake}}}^{t_{\text{sleep}}} V_{\text{in}} \cdot I(t)\, dt$$

k_timer_start(&tick_timer, K_USEC(10), K_USEC(10));

Generation and Analysis

a) Establish an SSH terminal session on the Debian environment running on the QRB2210 MPU. Run the standard workload generation tool stress-ng to load all CPU cores and memory channels:

stress-ng --cpu 4 --cpu-method all -io 4 \

--vm 2 --vm-bytes 128M -timeout 300s

b) Configure the oscilloscope to trigger on the rising edge of the signal on pin D2 with infinite persistence. Measure the peak-to-peak transition timing jitter:

$\Delta J = tedge, max - t_{edge, min}$ (5) over $_{10}{}^{6}$ continuous cycles.

The physical domain separation is validated if $_{\Delta J}$ remains within sub-microsecond levels, demonstrating that GPOS execution loads do not interfere with real-time operations.

Protocol 2: Power-Down-to-Data Latency and Energy Integration

Aim: Determine the energy footprint (E_{event}) and transition duration (T_{event}) during a low-power, sleepto-transmit transition.

5.2.1Test Setup and Instrumentation

a) Connect the board's main DC power line (VIN) to a Keysight N6705C DC Power Analyzer equipped with an N6781A Source/Measure Unit (SMU) to trace transient current draw ($_{I(t)}$) at a sampling rate of 100 kHz under a constant voltage V_{in} =

12.0 V.

b) Route a sync pin from the MCU (e.g., D3) to channel 2 of the power analyzer to record state changes.

5.2.2Test Sequence Steps

a) Place the board in low-power standby mode, with the MPU subsystem powered off.

b) Trigger a hardware wake-up event on the MCU via an external pin.

c) The MCU asserts the sync pin, activates the MPU power gate, and logs the timestamp.

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This test allows developers to evaluate battery life performance under different operational profiles.

Protocol 3: AI Inference Latency and Energy Efficiency Metrics

Aim: Compare the computational latency and energy efficiency of local neural network models across different execution units on the QRB2210.

Model and Environment Configuration

a) Deploy a standard Float32 MobileNetV2 image classification network (224 × 224 pixels) using a TensorFlow Lite runtime environment on the Debian Linux system.

b) Program the model to loop through 1,000 localized classification inferences.

5.3.2Execution Path Comparison

Execute the benchmarks across three distinct processing pathways on the QRB2210:

- **Execution Path A:** Multi-core execution on the Cortex-A53 CPU utilizing Arm Neon SIMD vector libraries.
- **Execution Path B:** GPU acceleration utilizing OpenCL compiler paths routed through the Adreno 702 core.
- **Execution Path C:** DSP hardware acceleration utilizing the Qualcomm Hexagon DSP pipeline.

5.3.3Comparative Metrics

For each execution path, record the average inference latency ($t_{inference}$) and determine the overall performance efficiency (η):

$$\eta = \frac{1}{\bar{P} \cdot t_{inference}} \quad \frac{inferences}{Joule} \qquad (7)$$

Where $\bar{P}$ is the average system power consumption measured by the DC power analyzer during active pipeline execution.

CONCLUSION

This paper presented a detailed architectural review, analytical model, and proposed experimental testing framework for the newly introduced Arduino UNO Q Single Board Computer. By separating tasks between a high-performance, Linux-capable Qualcomm QRB2210 MPU and an ultra-low-power, deterministic

STM32U585 MCU, the platform addresses the historic trade-off between compute capability and real-time responsiveness on a single board.

To support future performance evaluations of this platform, we established a formal Multi-Criteria Decision Analysis (MCDA) model to explain its coordinate positioning relative to alternative systems, and detailed three step-by-step, reproducible physical benchmarking protocols. By clearly separating verified hardware capabilities from proposed testing structures, this research provides a rigorous analytical baseline to support further empirical study and deployment of heterogeneous IoT edge devices.

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